

ELM623FA 20A Fully Integrated Synchronous Boost Converter

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■ General description

ELM623FA is a high efficiency fully integrated synchronous Boost converter with built-in main switch and synchronous switch. The device has 20A switch peak current capability and provides output voltage up to 18V. Synchronous rectification increases efficiency, reduces power losses and eases thermal requirements, allowing ELM623FA to be used in high power step-up applications. The 2.7V to 18V input voltage range supports a wide range of battery and AC powered inputs. The 70 μ A no load quiescent current extends operating run time in battery-powered systems. The operating frequency can be externally set for a 50kHz to 1MHz range, as for operation mode is automatic PSM/PWM mode. ELM623FA implements a programmable soft-start function, an adjustable cycle by cycle switching peak current limit function and thermal shutdown protection. ELM623FA is available in a small 20 pin 4mm \times 4mm QFN package.

■ Features

- Adjustable Input UVLO through EN pin
- Resistor or Inductor DCR current sensing
- Programmable Soft-start
- Cycle-by-Cycle Current Limit
- Thermal Shutdown
- Integrated 18V rating 9m Ω power switches with 20A peak current capability
- Input Range : 2.7V to 18.0V
- Output Voltage : 3.0V to 18.0V
- Low Quiescent Current : 70 μ A
- Low shutdown supply current : 3.5 μ A
- Adjustable Frequency : 50kHz to 1MHz
- Package : QFN20-4x4

■ Application

- USB Type C-PD and Thunderbolt Port for PCs
- Industrial Battery Powered POS Terminals
- Quick Charge Power Banks
- Electronic Cigarette
- Hi Power Bluetooth Speaker

■ Recommend operating conditions

Parameter	Symbol	Limit	Unit
Input Voltage	V _{in}	+2.7 to +18.0	V
Output Voltage	V _{out}	+3.0 to 18.0	V
Operating temperature	T _{op}	-40 to +85	°C

* Note: The device is not guaranteed to function outside of the recommended operating conditions.

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Maximum absolute ratings

Parameter	Symbol	Limit	Unit
VH to GND (Note 1)	Vvh	-0.3 to +20.0	V
ISP to GND (Note 1)	Visp		
ISN to GND (Note 1)	Visn		
OUT to GND (Note 1)	Vout		
ISP to ISN (Note 1)	Visp_isn	-0.3 to +0.3	V
PGND to GND (Note 1)	Vpgnd		
SW to GND (Note 1)	Vsw	-1 to Vout+1	V
Dynamic Vsw in 50ns duration (Note 1)		-3 to Vout+3	V
BST to SW (Note 1)	Vbst_sw	-0.3 to +6.0	V
EN to GND (Note 1)	Ven		
FB to GND (Note 1)	Vfb		
COMP to GND (Note 1)	Vcomp		
VCC to GND (Note 1)	Vcc		
Power dissipation at Ta=+25°C(Note 2, 3)	Pd	2.0	W
Storage temperature (Note 1)	Tstg	-55 to +150	°C

- * : 1. Stress exceeding those listed "Absolute maximum ratings" may damage the device.
 2. Measured on JESD51-7, 4-Layer PCB.
 3. The maximum allowable power dissipation is a function of the maximum junction temperature TJ_MAX, the junction to ambient thermal resistance θ_{ja} , and the ambient temperature Ta. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $Pd_{max} = (Tj_{max} - Ta) / \theta_{ja}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Selection Guide

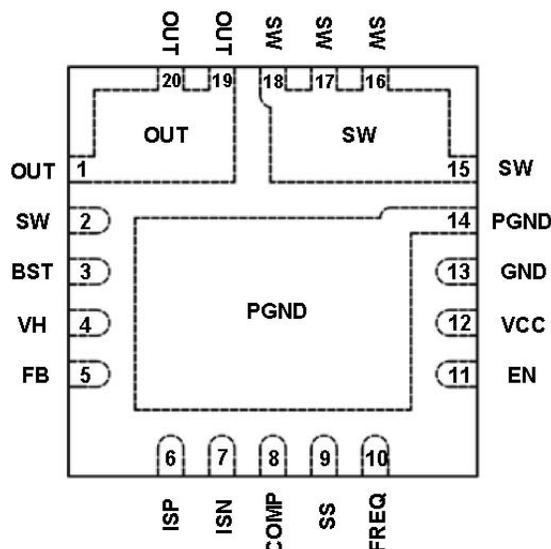
ELM623FA-N

Symbol		
a	Package	F: QFN20-4x4
b	Product version	A
c	Taping direction	N: Refer to PKG file

ELM623 F A - N
 ↑ ↑ ↑
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* Taping direction is one way.

Pin configuration



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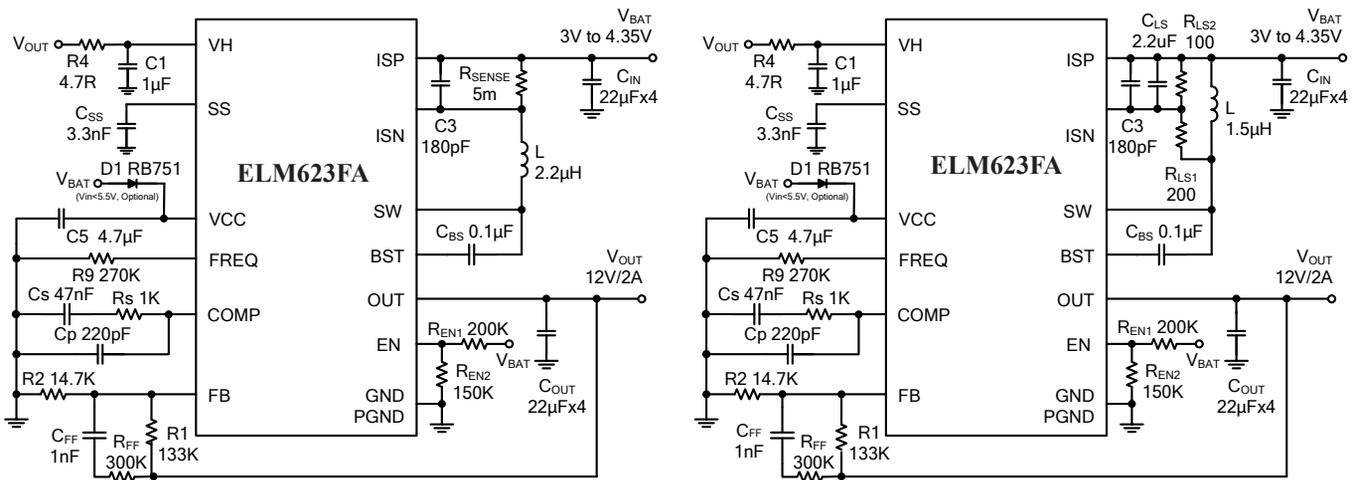
Pin description

Pin No.	Pin name	Description
1, 19, 20	OUT	Output of the Boost converter.
2, 15, 16, 17, 18	SW	Switching node of the Boost converter. Connect this pin to the inductor.
3	BST	Bootstrap capacitor node for Synchronous MOSFET. Connect the bootstrap capacitor 0.1 μ F from BST pin to the SW pin.
4	VH	The supply pin to On-Chip LDO Regulator. The operating voltage range on this pin is 2.7V to 18V (20V abs max). Bypass VH to PGND with a 0.1 μ F ceramic capacitor. When the input voltage V_{in} is < 5.5V, connect VH to the output of Boost converter to get maximum voltage for gate drivers. When the input voltage V_{in} is > 5.5V, connect VH to the input voltage to improve efficiency.
5	FB	Error amplifier input and feedback pin for output voltage regulation. Connect FB to the center tap of a resistor divider to set the output voltage.
6	ISP	Positive Current Sense Amplifier Input. The current sense resistor is normally placed at the input of the Boost converter in series with the inductor. The common mode voltage range on the ISP and ISN pins is 2.5V to 20V (20V Abs Max).
7	ISN	Negative Current Sense Amplifier Input.
8	COMP	Output of the internal transconductance error amplifier. The feedback loop compensation network is connected from COMP pin to GND.
9	SS	Soft-start programming pin. An external capacitor sets the ramp rate of the internal error amplifier's reference voltage during soft-start period. Typically connect SS to GND with a 3.3nF ceramic capacitor.
10	FREQ	Oscillator Frequency Set Input. A resistor from FREQ to GND sets the oscillator frequency from 50kHz to 1000kHz (Typical $R_{freq}=270k\Omega$ sets $F_{osc}=250kHz$). Leave this pin float to set 460kHz default frequency.
11	EN	Enable input. Pull EN above 1.22V to turn on the converter, and pull EN below 1.10V to shutdown the converter. EN pin can be used to implement externally adjustable input voltage under voltage lockout (UVLO) with two resistors. Connect EN to the center tap of a resistor divider to set the input UVLO threshold.
12	VCC	5.4V On-Chip Low Dropout Linear Regulator Output (LDO). This regulator powers all internal circuitry including the low side and high side N-channel MOSFET gate drivers. Bypass VCC to GND with a 1 μ F or greater ceramic capacitor. When the input voltage V_{in} is < 5.5V, Connect Vcc to V_{in} through a Diode.
13	GND	Signal Ground pin of the converter. All small-signal components and compensation components should be connected to this signal ground.
14	PGND	Power ground of the converter. It is connected to the source of the main MOSFET. Connect this pin to the (-) terminal(s) of C_{in} and C_{out} .

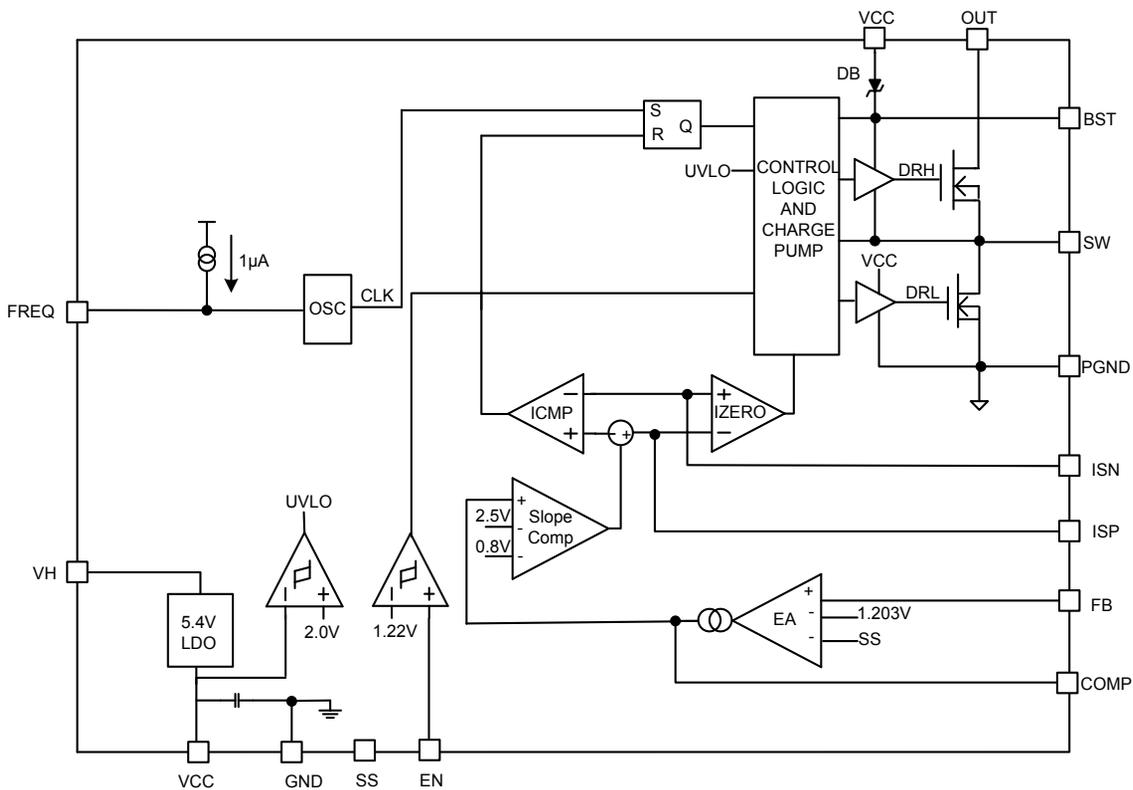
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Standard circuit



Block diagram



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■Electrical characteristics

Top=+25°C, Unless otherwise noted. Typical values are at Vh=12V, Visp=Visn=3.6V and Ven=2V.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply and enable						
Input supply voltage	Vh		2.7		18.0	V
Output voltage	Vout		3		18	V
Linear regulator output voltage	Vcc	6V<Vh<18V	5.1	5.4	5.7	V
Under-voltage lockout threshold	UVLO	Vh=Vcc Rising		2.0	2.5	V
		Vh=Vcc Falling		1.8		
EN Pin on threshold	Ven_on	Ven rising, turn on the device	1.120	1.220	1.320	V
EN Pin off threshold	Ven_off	Ven falling, turn off the device		1.10		V
EN Pin Input current	Ven_in	Ven=2V		100		nA
Operating quiescent current into VH	Ivh	Vfb=1.25V, Device no switching		70	100	μA
Shutdown current	Is	Ven=0V		3.5	10.0	μA
Error amplifier						
Feedback voltage	Vfb	PWM Mode	1.185	1.203	1.221	V
		Light load PSM mode		1.211		
Feedback Current	Ifb	Vfb=1.22V	-100	1	+100	nA
Error Amplifier Transconductance	Iea/Vtd	Vcomp=1.6V		1.3		mA/V
COMP pin clamp voltage	Vcomp	Hi Clamp voltage, VFB=1.1V		3.0		V
		Hi Clamp voltage, VFB=1.3V		0.4		
Current sense amplifier						
Maximum current sense threshold	Vmce	ΔV(isP-isN)	90	100	110	mV
Zero current sense threshold	Vzce	ΔV(isP-isN)		0		mV
ISP/ISN current sense input current	Iisp/isn	VisP=VisN=3.6V		10	20	μA
ISP/ISN current sense input range	Visp/isn		2.7		30.0	V
Oscillator frequency						
Oscillator frequency	Fosc	Rfreq=220kΩ	240	300	360	kHz
		Rfreq float		460		
Maximum duty cycle	Dmax			93		%
Minimum on time	Tmin			200		ns
Power switches						
Low side main switch on resistance	Rds(on)_L			9		mΩ
High side switch on resistance	Rds(on)_H			9		mΩ
Power switch leakage current	Ileak	Ven=0V, Vsw=18V and 0V		1	20	μA
Thermal shutdown						
Thermal shutdown threshold	Tsd			160		°C
Thermal shutdown hysteresis	Tsh			35		°C

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■ Detailed description (Refer to the functional block diagram)

ELM623FA is a fully-integrated synchronous boost converter with a 9mΩ synchronous switch to output. The device is capable of providing an output voltage up to 18V and delivering up to 25W power from a 2.7 V to 18V wide input. Voltage regulation is achieved employing constant frequency current mode pulse width modulation (PWM) control. The switching frequency is set either externally from 50kHz to 1MHz by an external timing resistor from FREQ pin to GND or default 460kHz by floating FREQ pin. The PWM control circuitry turns on the low side MOSFET at the beginning of each oscillator clock cycle, as the error amplifier compares the output voltage feedback signal at the FB pin to the internal 1.203V reference voltage. The low side MOSFET is turned-off when the inductor current reaches a threshold level set by the error amplifier output. After the low side MOSFET is turned off, the high side synchronous rectifier MOSFET is turned on until the beginning of the next oscillator clock cycle or until the inductor current reaches the zero current sense threshold. The input voltage is applied across the inductor and stores the energy as inductor current ramps up during the portion of the switching cycle when the low side MOSFET is on. Meanwhile the output capacitor supplies load current. When the low side MOSFET is turned off by the PWM comparator, the inductor transfers stored energy via the synchronous rectifier MOSFET to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The device skips pulse to improve efficiency at light load. In the light load mode, the converter only operates when the output voltage trips below a FB set threshold voltage 1.211V. It ramps up the output voltage with one or several pulses and skips pulse once the output voltage exceeds the set threshold voltage (PSM:Pulse Skipping Modulation). The devices feature internal slope compensation to avoid sub-harmonic oscillation that is intrinsic to peak current mode control at duty cycles higher than 50%. They also feature optional lossless inductor DCR current sensing, cycle-by-cycle current limit and over-temperature protection.

■ Application information

ELM623FA external component selection is driven by the load requirement, and begins with the selection of switching frequency, inductor and Rsense. Finally, input and output capacitors are selected.

■ Switching frequency selections

The first step is to determine the switching frequency of the Boost converter. There are tradeoffs to consider when selecting a higher or lower switching frequency. Typically, the designer uses the highest switching frequency possible since this results in the smallest solution size. A higher switching frequency allows for lower value inductors and smaller output capacitors compared to a Step-up converter that switches at a lower frequency. A lower switching frequency will produce a larger solution size but typically has a better efficiency by reducing MOSFET switching losses. The switching frequency is also limited by the minimum on-time of the converter based on the input voltage and the output voltage of the application. Minimum on-time, t_{ONmin} (200ns Typ.), is the smallest time duration that the ELM623FA is capable of turning on the low side MOSFET and correctly sensing inductor current for peak current mode control. To determine the maximum allowable switching frequency, first estimate the continuous conduction mode (CCM) duty cycle using Equation 1 with the maximum input voltage.

$$f_{osc(max)} = \frac{D(min)}{t_{on(min)}} = \frac{\frac{V_{out} - V_{in(max)}}{V_{out}}}{200ns} \quad (\text{Equation 1})$$

To determine the timing resistance at FREQ pin for a given switching frequency use the curve in Figure 1.

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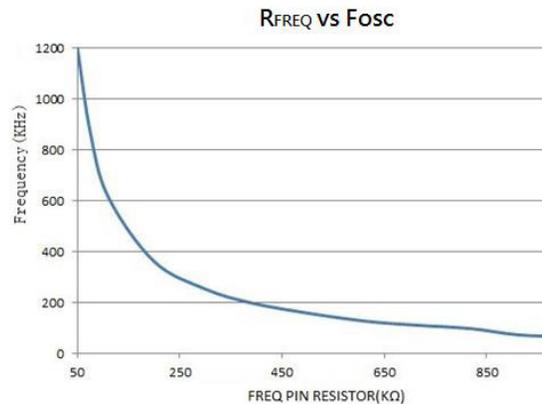


Figure 1. Switching frequency versus resistor value at the FREQ pin.

■ Input capacitor selection

Place a high quality 0.1μF in parallel with at least a 10μF or higher ceramic type X5R or X7R bypass capacitor at the VIN pin to power ground PGND for proper decoupling. Based on the application requirements additional bulk capacitance are needed to meet input voltage ripple, transient and EMI requirements. The value of the Cin is a function of the source impedance, and in general, the higher the source impedance, the larger input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current. The input capacitor voltage rating should exceed the maximum input voltage range.

■ Inductor selection

The selection of the inductor affects the steady-state operation as well as transient behavior and loop stability. These factors make it an important component in a switching power supply design. The three most important inductor specifications to consider are inductor value, DC resistance (DCR), and saturation current rating. In a step-up topology the average inductor current is equal to the input current. The highest average current through the inductor and the converter depends on the maximum output load, converter efficiency η , the minimum input voltage (V_{inmin}), and the output voltage (V_{out}). The inductor saturation current rating should be greater (by some margin) than the maximum average inductor current. Estimation of the maximum average inductor current can be done using Equation 2:

$$I_l(max) = I_{out(max)} \times \frac{V_{out}}{V_{in(min)} \times \eta} \quad (\text{Equation 2})$$

For example, for an output current of 2A at 12V with 90% efficiency, at least 8.9A of average current flows through the inductor at a minimum input voltage of 3V.

The inductor value has a direct effect on ripple current. Let the parameter ΔI_l represent the inductor peak-peak ripple current. The inductor ripple current contributes to the output current ripple that must be filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor. Higher values of ΔI_l lead to discontinuous mode (DCM) operation at moderate to light loads. The inductor ripple current ΔI_l decreases with higher inductance or frequency and increases with higher V_{in} . Estimation of the inductor ripple current can be done using Equation 3:

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$$\Delta I_l = \frac{V_{in}}{f_{osc} \cdot L} \left(1 - \frac{V_{in}}{V_{out}} \right) \quad (\text{Equation 3})$$

Accepting larger values of ΔI_l allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_l = 0.3 \sim 0.5 \cdot I_{lmax}$.

ELM623FA Boost converters have been optimized to operate with an effective inductance in the range of 1 μ H to 10 μ H. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions.

■ISP and ISN pins

ELM623FA can use either a discrete sense resistor (R_{sense}) or inductor DCR (DC resistance) sensing for current sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the converter.

The ISP and ISN pins are the inputs to the current sense amplifier. The common mode input voltage range of the current sense amplifier is 2.7V to 18V. The current sense resistor is normally placed at the input of the converter in series with the inductor. The ISP pin also provides power to the current comparator. ISP draws approximately 10~30 μ A during normal operation. There is a typical 10 μ A bias current that flows into the ISN pin. The sense lines should be Kelvin-sense connection underneath the current sense resistor (shown in Figure 2). If inductor DCR sensing is used (Figure 3b), sense resistor R1 should be placed close to the switching node, and the mutual filter capacitor C1 should be placed close to the ELM623FA to prevent noise from coupling into sensitive small-signal nodes.

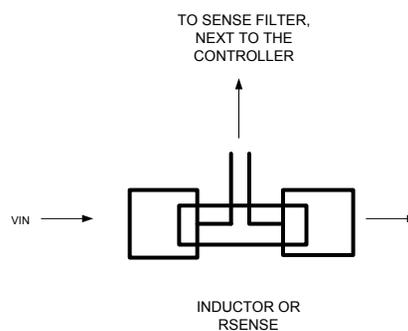
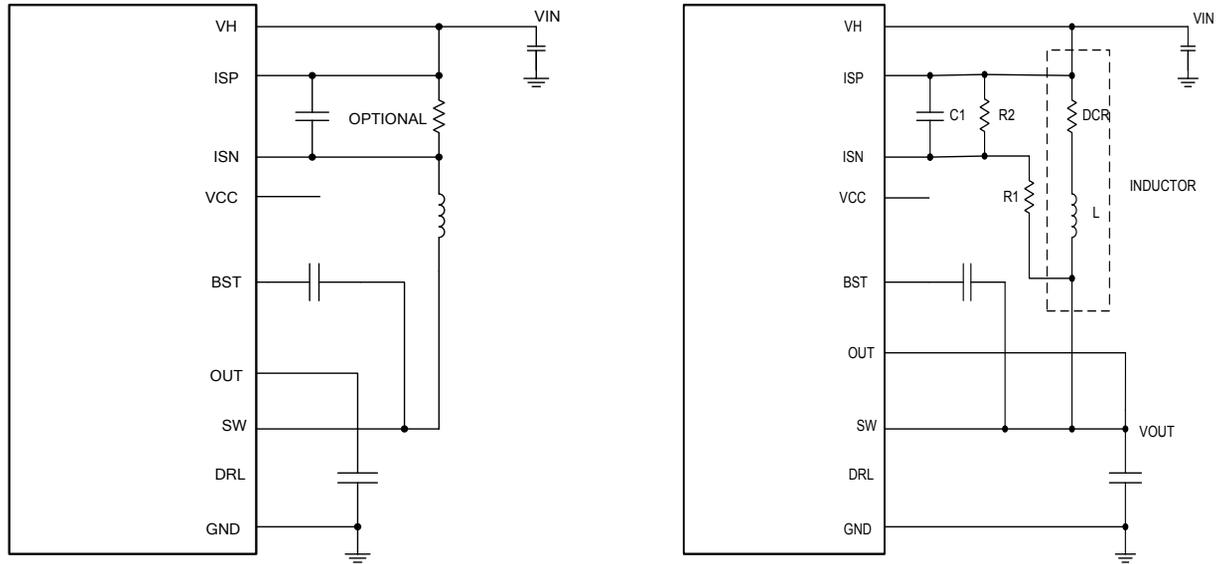


Figure 2. Sense lines placement with inductor or sense resistor.

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(3a) Using a current sense resistor.

(3b) Using the inductor DCR to sense current.

Figure 3. Two current sensing methods.

■ Current sensing resistor

A typical sensing circuit using a discrete resistor is shown in Figure 3a. R_{sense} is chosen based on the required maximum average inductor current. The current comparator has a maximum threshold $V_{sensemax}$ of 100mV (typical) and 90mV (minimum). To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value 92mV for the maximum current sense threshold $V_{sensemax}$. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, I_{lmax} , equal to the peak value less half the peak-to-peak ripple current, ΔI_l . To calculate the sense resistor value, use the Equation 4:

$$R_{sense} = \frac{V_{sensemax}}{I_{lmax} + \frac{\Delta I_l}{2}} = \frac{90mV}{I_{lmax} + \frac{\Delta I_l}{2}} \quad (\text{Equation 4})$$

R_{sense} also affects the current mode control loop gain. Choose R_{sense} in the 3~20m Ω range.

■ Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, ELM623FA is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 3b. The DCR sensing reduces conduction loss through a sense resistor and improve efficiency by a few percent. A flat frequency response is achieved when the inductor time constant matches that of the RC sense network. If the external $R1||R2 \cdot C1$ time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by $R2/(R1+R2)$. $R2$ scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. The DCR of the inductor can be less than 5m Ω for high current inductors, and the $R2$ resistor is not used. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturer's data sheets for

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detailed information. Using the inductor ripple current value from the inductor section, the equivalent sense resistor value is calculated with Equation 5:

$$R_{\text{sense(equiv)}} = \text{DCR} \cdot \frac{R_2}{R_1 + R_2} = \frac{V_{\text{sensemin}}}{I_{\text{imax}} + \frac{\Delta I_L}{2}} = \frac{90\text{mV}}{I_{\text{imax}} + \frac{\Delta I_L}{2}} \quad (\text{Equation 5})$$

Choose $R_1 \parallel R_2$ around 200Ω to reduce error due to the ISN pin $10\mu\text{A}$ (Typical) input bias current. C_1 is calculated by Equation 6 and usually selected to be in the range of 100nF to $10\mu\text{F}$.

$$C_1 = \frac{L}{\text{DCR} \cdot R_1 \parallel R_2} = \frac{L}{\text{DCR}} \cdot \frac{R_1 + R_2}{R_1 \cdot R_2} \quad (\text{Equation 6})$$

■ Setting input under-voltage lockout (UVLO)

The EN pin voltage must be greater than 1.22V (typical) to enable ELM623FA. The device enters shutdown mode when the EN voltage is less than 1.10V . In shutdown mode, the input supply current for the device is less than $5\mu\text{A}$. When the EN pin voltage is higher than the shutdown threshold but less than 1.22V , the devices are in standby mode. Adjustable input UVLO can be accomplished using the EN pin. As shown in Figure 4, a resistor divider from the VIN pin to GND sets the input UVLO level. Choose the bottom UVLO resistor $R_{\text{uvlo_bot}}$ in the $10\text{k}\Omega \sim 200\text{k}\Omega$ range to set the divider current at $10\mu\text{A}$ or higher. Typically select $R_{\text{uvlo_bot}} = 100\text{k}\Omega$. The value of top resistor $R_{\text{uvlo_top}}$, depending on the the desired turn-on voltage V_{start} at the VIN pin, can be calculated with Equation 7:

$$R_{\text{uvlo_top}} = R_{\text{uvlo_bot}} \times \left(\frac{V_{\text{start}}}{V_{\text{en}}} - 1 \right) = 100\text{k}\Omega \times \left(\frac{V_{\text{start}}}{1.22\text{V}} - 1 \right) \quad (\text{Equation 7})$$

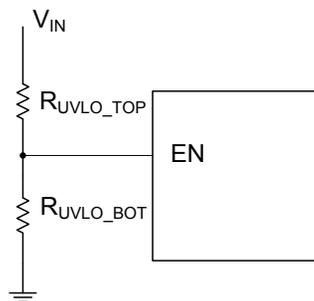


Figure 4. Input UVLO setting.

■ Bootstrap capacitor selection

Place a $10\text{nF} \sim 0.1\mu\text{F}$ X5R or X7R ceramic capacitor between BST and SW pins for the proper operation. This capacitor provides gate drive voltage to turn on the high-side MOSFET.

■ VCC Low-dropout linear regulator

ELM623FA features an internal P-channel low dropout linear regulator (LDO) that supplies power to the VCC pin from the VH supply pin. VCC powers the gate drivers and ELM623FA's internal circuitry. The LDO output VCC is regulated to 5.4V . It can supply at least 20mA and must be bypassed to ground with $1\mu\text{F} \sim 4.7\mu\text{F}$ X5R or better grade ceramic capacitor. The capacitor should have a 10V or higher voltage rating. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. A VCC under-voltage detection

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circuit prevents the internal PWM control circuitry and power switches from operation when VCC voltage is below 2V (typical).

■ Output capacitor selection

In a step-up converter, the output has a discontinuous current, so output capacitor C_{out} must be capable of reducing the output voltage ripple and filtering the high di/dt path of the supply. It is recommended to use X5R or X7R ceramic capacitors placed as close as possible to the VOUT pin and power ground PGND pin. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple voltage due to charging and discharging the bulk output capacitance in a single phase step-up converter is given by Equation 8. This value does not take into account the ESR of the output capacitor.

$$\Delta V_{out} = \frac{I_{outmax} \times D_{max}}{C_{out} \times f_{osc}} = \frac{I_{out(max)} \times \frac{V_{out} - V_{in(min)}}{V_{out}}}{C_{out} \times f_{osc}} \quad (\text{Equation 8})$$

Where C_{out} is the output filter capacitor.

For example: Build 5V nominal output voltage from the minimum 3V input supply voltage. Select switching frequency 600kHz. Choose output capacitor to get less than 50mV ripple (1% of V_{out}) at maximum 4Amp output current. The minimum output capacitor is 53 μ F required to limit the output voltage ripple.

$$C_{out} \geq \frac{I_{outmax} \times D_{max}}{\Delta V_{out} \times f_{osc}} = \frac{4A \times \frac{5V - 3V}{5V}}{5V \times 1\% \times 600kHz} = 53\mu F \quad (\text{Equation 9})$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Ceramic capacitors have excellent low ESR characteristics but can have a DC Bias effect, which will have a strong influence on the final effective capacitance. Capacitance deratings for aging, temperature and dc bias increase the minimum value required. The voltage rating must be greater than the output voltage with some tolerance for output voltage ripple and overshoot in transient conditions. For this example 4 \times 22 μ F, 25V ceramic capacitors with 5m Ω of ESR are used. The 40% derated capacitance is 52.8 μ F, approximately equal to the calculated minimum.

■ Setting output voltage

ELM623FA output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also, keep the FB trace as short as possible to avoid noise pickup. The typical value of the voltage on the FB pin is 1.203V. The maximum allowed value for the output voltage is 18V. Choose the bottom resistor R_{fb_bot} in the 10k Ω ~200k Ω range to set the divider current at 6 μ A or higher. Typically select R_{fb_bot} =100k Ω . The value of top resistor R_{fb_top} , depending on the needed output voltage V_{out} , can be calculated using Equation 10:

$$R_{fb_top} = R_{fb_bot} \times \left(\frac{V_{out}}{V_{fb}} - 1 \right) = 100k\Omega \times \left(\frac{V_{out}}{1.203V} - 1 \right) \quad (\text{Equation 10})$$

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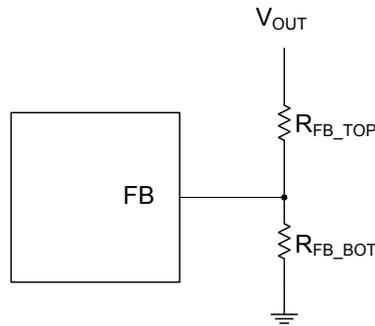


Figure 5. Output voltage setting.

■ The control loop compensation

The series Rc-Cc filter at COMP pin sets the dominant pole-zero loop compensation. The resistor Rc in series with a capacitor Cc creates a compensating zero. A capacitor Cc1 in parallel to these two components can be added to form a compensating pole. In a step-up topology, the maximum crossover frequency is typically limited by the right-half plane zero (RHPZ). The compensation design should be done at the minimum input voltage and full load when the RHPZ is at the lowest frequency. The crossover frequency should also be limited to less than 1/4 of the RHPZ frequency.

Table 1. Gives Rc, Cc and Cc1 values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher Rc value can be used to enlarge the bandwidth, as well as a slightly lower value of Cc to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of ELM623FA.

Table 1. Recommended compensation network values.

Application	I _{out_max}	F _{sw}	Inductor	R _{sense}	C _{in}	C _{out}	Rc	Cc and Cc1
1-Cell step-up to 5V Vin range: 3V~4.35V	5A	250kHz	1.5μH Isat=18A	5mΩ	4*22μF 16V	4*22μF 16V	1kΩ	Cc=47nF Cc1=220pF
1-Cell step-up to 9V Vin range: 3V~4.35V	3A	250kHz	1.5μH Isat=18A	5mΩ	4*22μF 25V	4*22μF 25V	1kΩ	Cc=47nF Cc1=220pF
1-Cell step-up to 12V Vin range: 3V~4.35V	2A	250kHz	1.5μH Isat=18A	5mΩ	4*22μF 25V	4*22μF 25V	1kΩ	Cc=47nF Cc1=220pF
2-Cell step-up to 12V Vin range: 6V~8.40V	2A	250kHz	1.5μH Isat=18A	5mΩ	4*22μF 25V	4*22μF 25V	1kΩ	Cc=47nF Cc1=220pF

■ Thermal information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design
- Improve the thermal coupling of the component to the PCB
- Introducing airflow in the system

ELM623FA 20A Fully Integrated Synchronous Boost Converter

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The maximum junction temperature (T_j) of the ELM623FA device is 160°C and worst case won't exceed 145°C . The thermal resistance of the 20-pin QFN package is $\theta_{ja} = 50^\circ\text{C/W}$, if the Exposed PAD is soldered. Specified regulator operation is assured to a maximum ambient temperature T_a of $+85^\circ\text{C}$. Therefore, the maximum power dissipation for the 20-pin QFN package is about 1W. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_d(\text{max}) = \frac{T_j(\text{max}) - T_a}{\theta_{ja}} = \frac{145^\circ\text{C} - 85^\circ\text{C}}{50^\circ\text{C/W}} = 1.2\text{W} \quad (\text{Equation 11})$$

Layout consideration

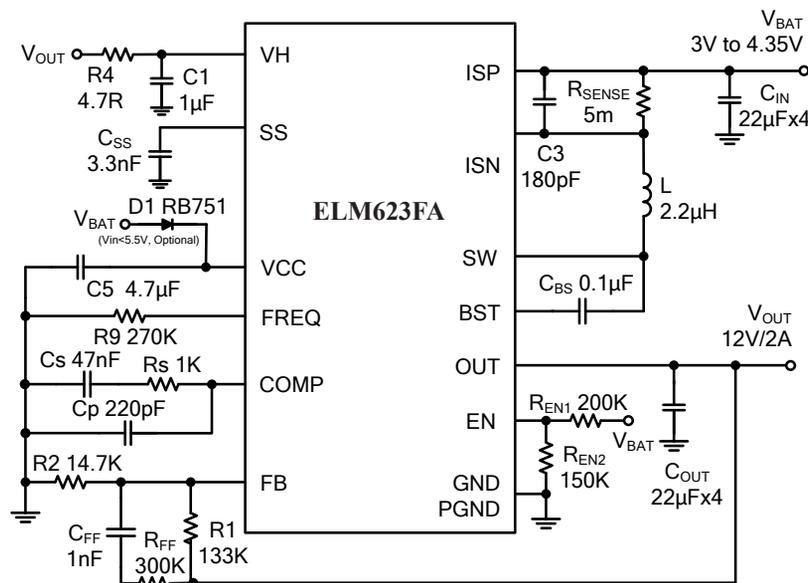
For designing ELM623FA a boost power supply, especially those operating at high output voltage and current application, PCB layout is a very important in design step. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin to reducing the high frequency noise of coupling to GND plane to cause EMI or power system unstable.

Check the following layout rules:

1. Put the input capacitors GND, output capacitors GND and the PGND of ELM623FA in the same of power plane to reduce impedance to avoid EMI and increase efficiency of power system.
2. The GND and PGND kept separate and used dot short skill to avoid noise coupling to GND to cause power system unstable as ELM623FA EV board PCB design.
3. ISP and ISN trace routing like a differential pair to shielding each other to filter the common mode noise. And far away the SW trace to avoid to be coupled that will cause the current limit protection circuit fault. Ensure accurate current sensing with Kelvin connections at the sense resistor or the DCR of inductor.
4. Keep the switching node (SW and PGND) and boost node (BST) away from sensitive small-signal nodes.

Application schematic

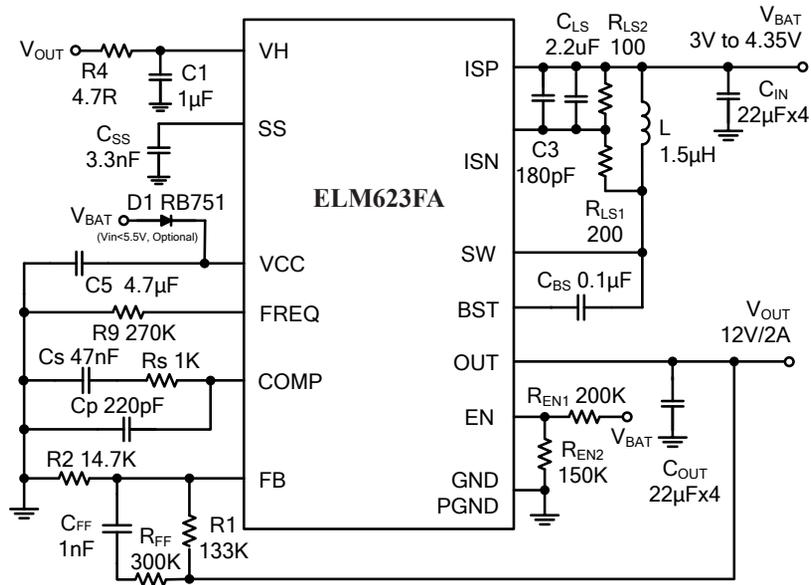
- 1-Cell Application:



Current sensing resistor

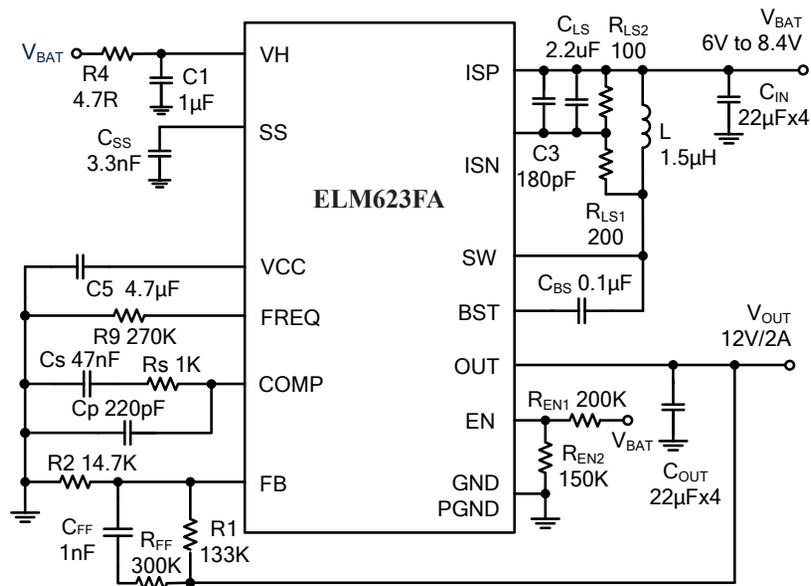
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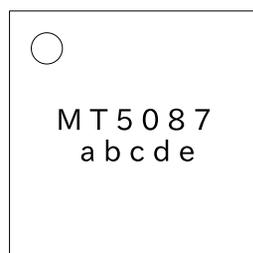
Current sensing DCR of inductor

• 2-Cell Application:



Current sensing DCR of inductor

■ Marking



Mark	Content
MT5087	Product code
a to e	Lot No.

ELM623FA 20A Fully Integrated Synchronous Boost Converter

<https://www.elm-tech.com>

EVB BOM List

Qty	Ref	Value	Description	Package	
4	Cin	22 μ F	Ceramic capacitor, 16V, X5R	0805	
4	Cout	22 μ F	Ceramic capacitor, 30V, X5R	0805	
1	L	1.5 μ H for L sense 2.2 μ H for R sense	MHC106030-1R5M-R8, 15m Ω , 18A(SAT), 9.5A(RMS) MHC106030-2R2M-R8, 20m Ω , 14A(SAT), 8.5A(RMS)	SMD	
1	R1	133k Ω	Resistor, \pm 1%	0603	
1	R2	Vout=5V	42.2k Ω	Resistor, \pm 1%	0603
		Vout=9V	20.5k Ω		
		Vout=12V	14.7k Ω		
		Vout=20V	8.45k Ω		
1	Rff	300k Ω	Resistor, \pm 5%	0603	
1	R4	4.7 Ω	Resistor, \pm 5%	0603	
1	Rs	1k Ω	Resistor, \pm 1%	0603	
1	Ren1	156k Ω	Resistor, \pm 5%	0603	
1	Ren1	200k Ω	Resistor, \pm 5%	0603	
1	Ren2	150k Ω	Resistor, \pm 5%	0603	
1	R9	270k Ω	Resistor, \pm 5%	0603	
1	Rsense	5m Ω	Resistor, \pm 1%	1206	
1	Rls1	200 Ω	Resistor, \pm 1%	0603	
1	Rls2	100 Ω	Resistor, \pm 1%	0603	
1	C1	1 μ F	Ceramic capacitor, 10V, X5R	0603	
1	C3	180pF	Ceramic capacitor, 10V, X5R	0603	
1	C5	4.7 μ F	Ceramic capacitor, 10V, X5R	0603	
1	Cff	1nF	Ceramic capacitor, 10V, X5R	0603	
1	Css	3.3nF	Ceramic capacitor, 10V, X5R	0603	
1	Cbs	0.1 μ F	Ceramic capacitor, 10V, X5R	0603	
1	Cls	2.2 μ F	Ceramic capacitor, 10V, X5R	0603	
1	CS	47nF	Ceramic capacitor, 10V, X5R	0603	
1	CP	220pF	Ceramic capacitor, 10V, X5R	0603	
1	D1	RB751	Diode, RB751		
1	Power IC	ELM623FA	Boost DC/DC converter	QFN20-4x4	