

Single N-channel MOSFET

ELM4NS6032FAA-N

<http://www.elm-tech.com>

■ General description

ELM4NS6032FAA-N uses advanced trench technology to provide excellent $R_{ds(on)}$, low gate charge and low gate threshold voltage.

■ Features

- $V_{ds}=60V$
- $I_d=13A$ ($V_{gs}=10V$)
- $R_{ds(on)} = 8.5m\Omega$ ($V_{gs}=10V$)
- $R_{ds(on)} = 12.0m\Omega$ ($V_{gs}=4.5V$)

■ Maximum absolute ratings

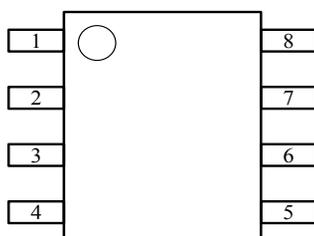
| Parameter | Symbol | Limit | Unit | Note | |
|--|-----------|-------------------|------------|------|------------------|
| Drain-source voltage | V_{ds} | 60 | V | | |
| Gate-source voltage | V_{gs} | ± 20 | V | | |
| Continuous drain current ($V_{gs}=10V$) | I_d | $T_a=25^\circ C$ | 13 | A | 1 |
| | | $T_a=100^\circ C$ | 8 | | |
| Pulsed drain current | I_{dm} | 60 | A | 2 | |
| Single pulse avalanche energy | EAS | 80 | mJ | 3 | |
| Avalanche current | I_{as} | 40 | A | | |
| Power dissipation | P_d | 2.7 | W | 4 | |
| | | | | | $T_a=25^\circ C$ |
| Storage temperature range | T_{stg} | - 55 to 150 | $^\circ C$ | | |
| Operating junction temperature range | T_j | - 55 to 150 | $^\circ C$ | | |

■ Thermal characteristics

| Parameter | Symbol | Typ. | Max. | Unit | Note | |
|--|--------------|-----------------|------|------|--------------|---|
| Thermal resistance junction-to-ambient | $t \leq 10s$ | $R_{\theta ja}$ | - | 45 | $^\circ C/W$ | 1 |
| | Steady state | $R_{\theta ja}$ | - | 80 | | 1 |

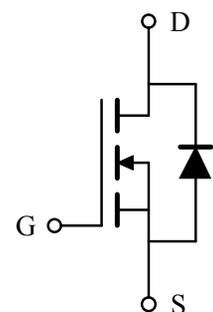
■ Pin configuration

SOP-8(TOP VIEW)



| Pin No. | Pin name |
|---------|----------|
| 1 | SOURCE |
| 2 | SOURCE |
| 3 | SOURCE |
| 4 | GATE |
| 5 | DRAIN |
| 6 | DRAIN |
| 7 | DRAIN |
| 8 | DRAIN |

■ Circuit



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■Electrical characteristics

T_j=25°C. Unless otherwise noted.

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|-----------------------------------|---------------------|---|------------------------------------|------|------|------|------|
| STATIC PARAMETERS | | | | | | | |
| Drain-source breakdown voltage | BV _{dss} | I _d =250μA, V _{gs} =0V | 60 | - | - | V | |
| Drain-source leakage current | I _{dss} | V _{ds} =48V V _{gs} =0V | - | - | 1 | μA | |
| | | T _j =55°C | - | - | 5 | | |
| Gate-body leakage current | I _{gss} | V _{ds} =0V, V _{gs} =±20V | - | - | ±100 | nA | |
| Gate threshold voltage | V _{gs(th)} | V _{ds} =V _{gs} , I _d =250μA | 1.2 | - | 2.5 | V | |
| Static drain-source on-resistance | R _{ds(on)} | V _{gs} =10V, I _d =10A | - | - | 8.5 | mΩ | 2 |
| | | V _{gs} =4.5V, I _d =8A | - | - | 12.0 | | |
| Forward transconductance | G _{fs} | V _{ds} =5V, I _d =10A | - | 50 | - | S | |
| Diode forward voltage | V _{sd} | I _s =1A, V _{gs} =0V | - | - | 1.2 | V | 2 |
| Diode continuous source current | I _s | V _{gs} =V _{ds} =0V, Force current | - | - | 10 | A | 1, 5 |
| Pulsed source current | I _{sm} | | - | - | 60 | A | 2, 5 |
| DYNAMIC PARAMETERS | | | | | | | |
| Input capacitance | C _{iss} | V _{gs} =0V, V _{ds} =25V, f=1MHz | - | 3307 | - | pF | |
| Output capacitance | C _{oss} | | - | 201 | - | pF | |
| Reverse transfer capacitance | C _{rss} | | - | 151 | - | pF | |
| SWITCHING PARAMETERS | | | | | | | |
| Total gate charge (10V) | Q _g | V _{gs} =10V, V _{ds} =48V I _d =10A | - | 57.0 | - | nC | |
| Gate-source charge | Q _{gs} | | - | 8.7 | - | nC | |
| Gate-drain charge | Q _{gd} | | - | 14.0 | - | nC | |
| Turn-on delay time | t _{d(on)} | V _{gs} =10V, V _{ds} =30V I _d =10A, R _{gen} =3.3Ω | - | 16.2 | - | ns | |
| Turn-on rise time | t _r | | - | 41.2 | - | ns | |
| Turn-off delay time | t _{d(off)} | | - | 56.4 | - | ns | |
| Turn-off fall time | t _f | | - | 16.2 | - | ns | |
| Reverse recovery time | t _{rr} | | I _f =10A, di/dt=100A/μs | - | 24.0 | - | ns |
| Reverse recovery charge | Q _{rr} | - | | 15.0 | - | nC | |

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows Max. rating . The test condition is V_{dd}=50V, V_{gs}=10V, L=0.1mH, I_{as}=40A.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_d and I_{dm}, in real applications, should be limited by total power dissipation.

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■ Typical electrical and thermal characteristics

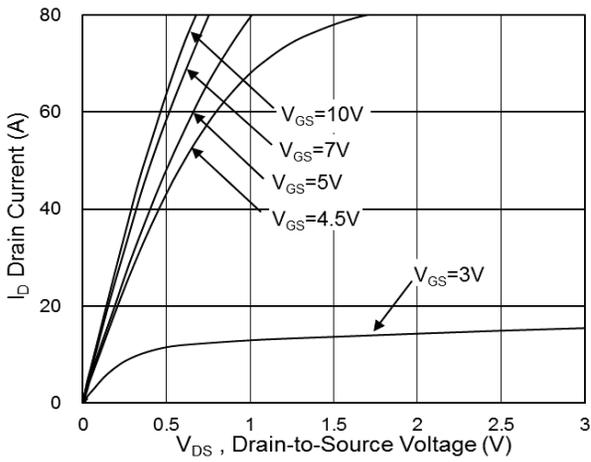


Fig.1 Typical Output Characteristics

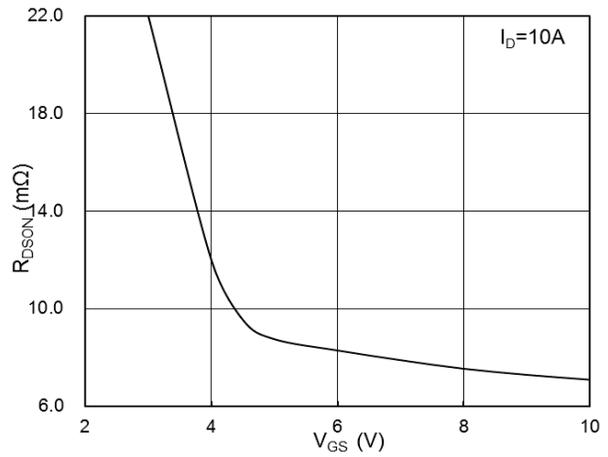


Fig.2 On-Resistance v.s Gate-Source Voltage

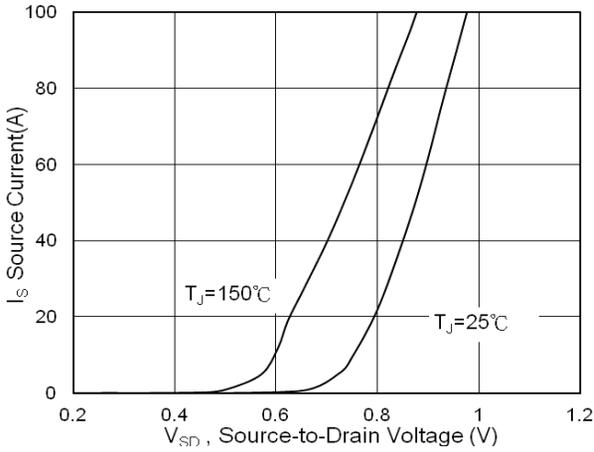


Fig.3 Forward Characteristics of Reverse

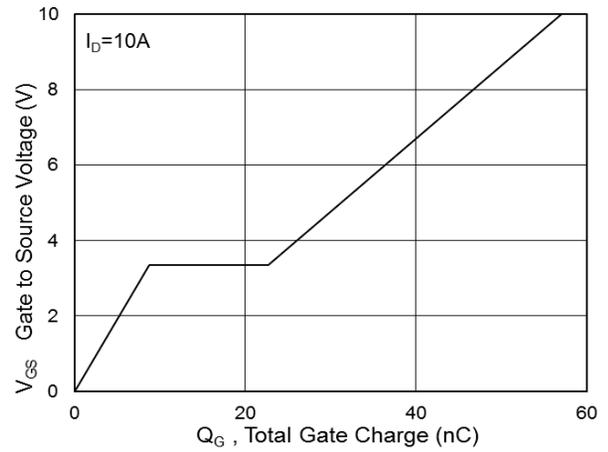


Fig.4 Gate-Charge Characteristics

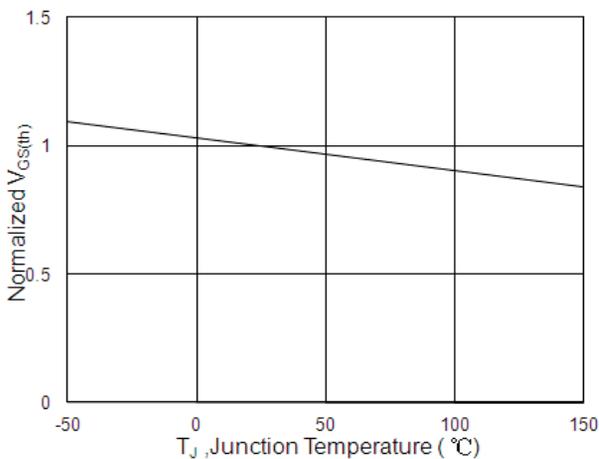


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

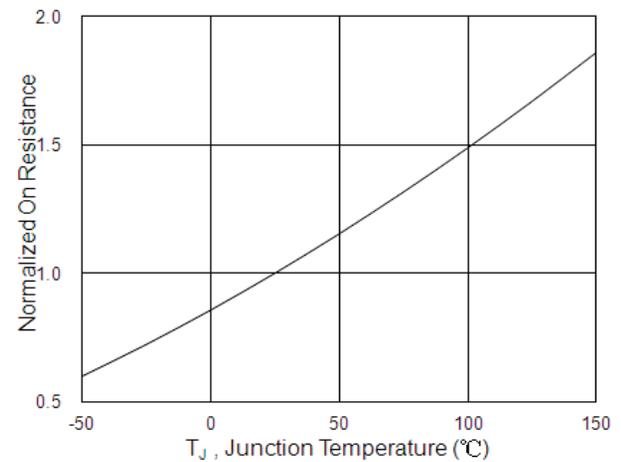


Fig.6 Normalized R_{DSON} vs. T_J

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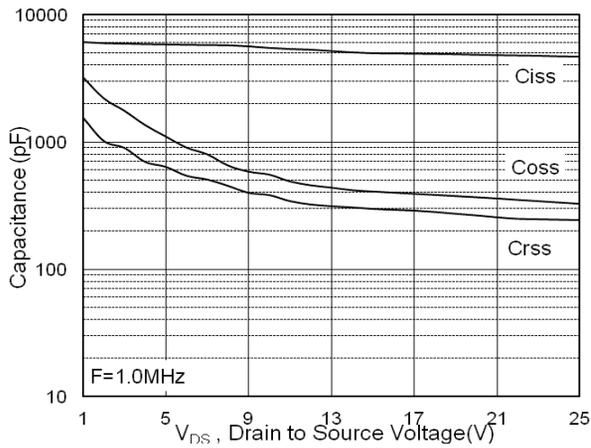


Fig.7 Capacitance

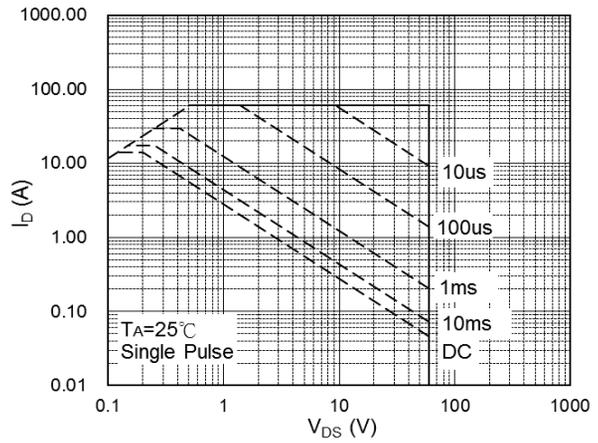


Fig.8 Safe Operating Area

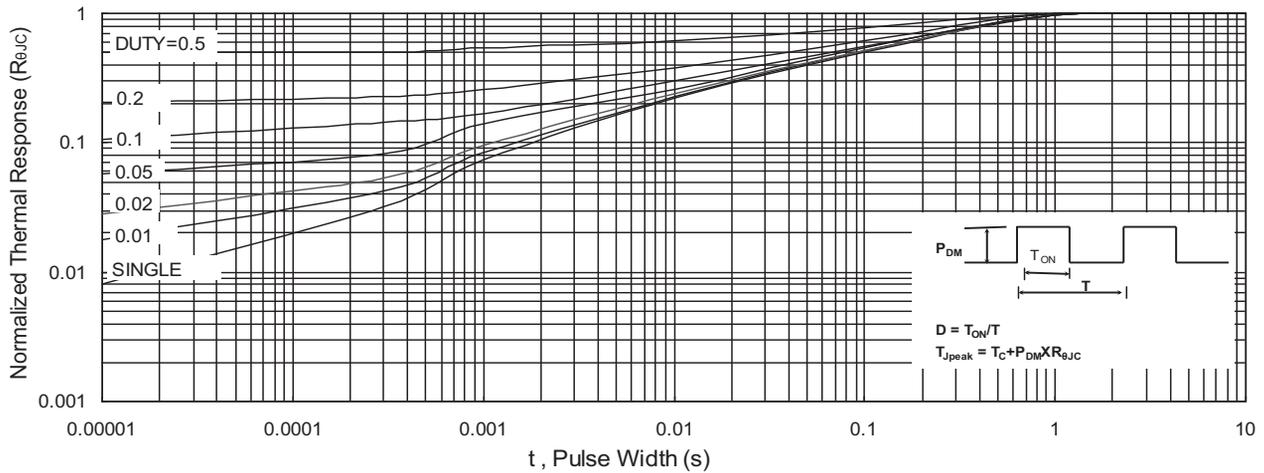


Fig.9 Normalized Maximum Transient Thermal Impedance

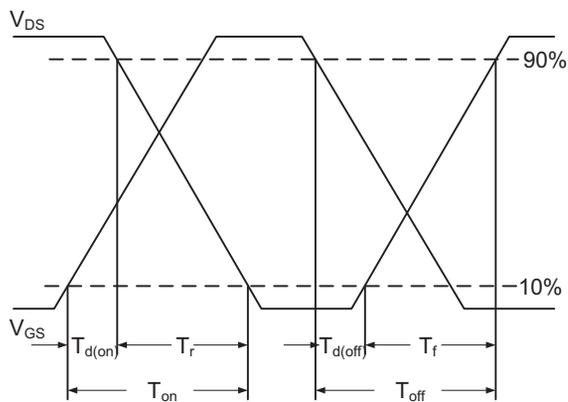


Fig.10 Switching Time Waveform

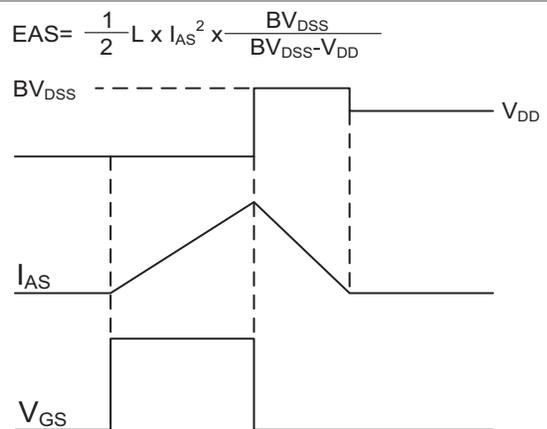


Fig.11 Unclamped Inductive Switching Waveform