

# Single P-channel MOSFET

## ELM4P2607FAA-S

<http://www.elm-tech.com>

### ■ General description

ELM4P2607FAA-S uses advanced trench technology to provide excellent  $R_{ds(on)}$ , low gate charge and low gate threshold voltage.

### ■ Features

- $V_{ds} = -20V$
- $I_d = -6.9A$  ( $V_{gs} = -4.5V$ )
- $R_{ds(on)} = 30m\Omega$  ( $V_{gs} = -4.5V$ )
- $R_{ds(on)} = 38m\Omega$  ( $V_{gs} = -2.5V$ )
- $R_{ds(on)} = 55m\Omega$  ( $V_{gs} = -1.8V$ )

### ■ Maximum absolute ratings

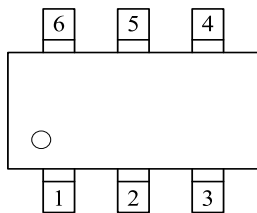
Parameter	Symbol	Limit	Unit	Note	
Drain-source voltage	$V_{ds}$	-20	V		
Gate-source voltage	$V_{gs}$	$\pm 12$	V		
Continuous drain current ( $V_{gs} = -4.5V$ )	$I_d$	$T_a = 25^\circ C$	-6.9	A	1
		$T_a = 70^\circ C$	-5.4		
Pulsed drain current	$I_{dm}$	-20	A	2	
Power dissipation	$P_d$	1.0	W	3	
Junction and storage temperature range	$T_j, T_{stg}$	-55 to +150	$^\circ C$		

### ■ Thermal characteristics

Parameter	Symbol	Typ.	Max.	Unit	Note
Thermal resistance junction-to-ambient	$R_{\theta ja}$	-	50	$^\circ C/W$	1
Thermal resistance junction-to-ambient		-	100		

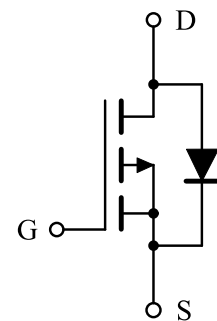
### ■ Pin configuration

TSOP-6(TOP VIEW)



Pin No.	Pin name
1	DRAIN
2	DRAIN
3	GATE
4	SOURCE
5	DRAIN
6	DRAIN

### ■ Circuit



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### ■ Electrical characteristics

T<sub>j</sub>=25°C. Unless otherwise noted.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
<b>STATIC PARAMETERS</b>							
Drain-source breakdown voltage	BV <sub>dss</sub>	V <sub>gs</sub> =0V, I <sub>d</sub> =-250μA	-20	-	-	V	
Zero gate voltage drain current	I <sub>dss</sub>	V <sub>ds</sub> =-16V, V <sub>gs</sub> =0V	-	-	-1	μA	
		V <sub>ds</sub> =-16V, V <sub>gs</sub> =0V, T <sub>j</sub> =55°C	-	-	-5		
Gate-body leakage current	I <sub>gss</sub>	V <sub>ds</sub> =0V, V <sub>gs</sub> =±12V	-	-	±100	nA	
Gate threshold voltage	V <sub>gs(th)</sub>	V <sub>ds</sub> =V <sub>gs</sub> , I <sub>d</sub> =-250μA	-0.3	-0.5	-1.0	V	
Static drain-source on-resistance	R <sub>ds(on)</sub>	V <sub>gs</sub> =-4.5V, I <sub>d</sub> =-4.0A	-	25	30	mΩ	2
		V <sub>gs</sub> =-2.5V, I <sub>d</sub> =-2.0A	-	32	38		
		V <sub>gs</sub> =-1.8V, I <sub>d</sub> =-1.5A	-	42	55		
Forward transconductance	G <sub>fs</sub>	V <sub>ds</sub> =-5V, I <sub>d</sub> =-4A	-	21	-	S	
Diode forward voltage	V <sub>sd</sub>	I <sub>s</sub> =-1A, V <sub>gs</sub> =0V	-	-	-1	V	2
Max. body-diode continuous current	I <sub>s</sub>	V <sub>gs</sub> =V <sub>ds</sub> =0V, Force Current	-	-	-6.9	A	1, 4
Pulsed source current	I <sub>sm</sub>		-	-	-18.8	A	2, 4
<b>DYNAMIC PARAMETERS</b>							
Input capacitance	C <sub>iss</sub>	V <sub>gs</sub> =0V, V <sub>ds</sub> =-15V, f=1MHz	-	2280	-	pF	
Output capacitance	C <sub>oss</sub>		-	220	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>		-	187	-	pF	
<b>SWITCHING PARAMETERS</b>							
Total gate charge (-4.5V)	Q <sub>g</sub>	V <sub>gs</sub> =-4.5V, V <sub>ds</sub> =-15V I <sub>d</sub> =-4A	-	27.3	-	nC	
Gate-source charge	Q <sub>gs</sub>		-	3.6	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	6.5	-	nC	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>gs</sub> =-4.5V, V <sub>ds</sub> =-10V I <sub>d</sub> =-4A, R <sub>gen</sub> =3.3Ω	-	9.2	-	ns	
Turn-on rise time	t <sub>r</sub>		-	59.0	-	ns	
Turn-off delay time	t <sub>d(off)</sub>		-	99.0	-	ns	
Turn-off fall time	t <sub>f</sub>		-	71.0	-	ns	
Reverse recovery time	t <sub>rr</sub>	I <sub>f</sub> =-4A, dI/dt=100A/μs	-	52	-	nS	
Reverse recovery charge	Q <sub>rr</sub>		-	28	-	nC	

#### NOTE :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs and duty cycle ≤ 2%.
3. The power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as I<sub>d</sub> and I<sub>dm</sub>, in real applications, should be limited by total power dissipation.

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## ■ Typical electrical and thermal characteristics

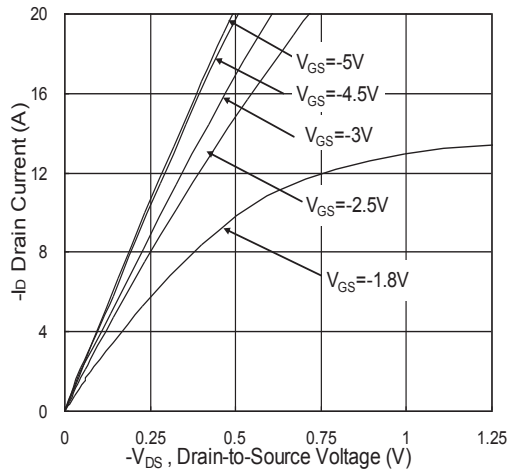


Fig.1 Typical Output Characteristics

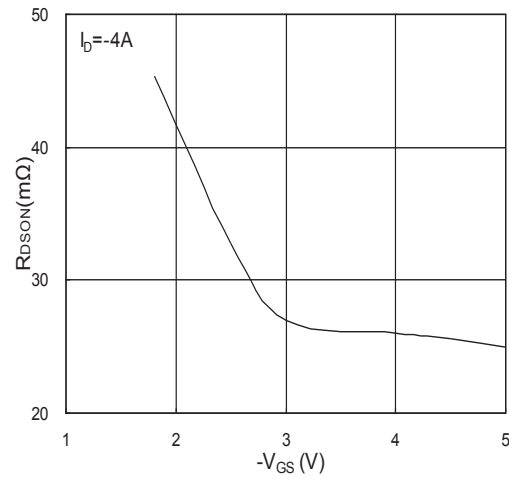


Fig.2 On-Resistance vs. Gate-Source

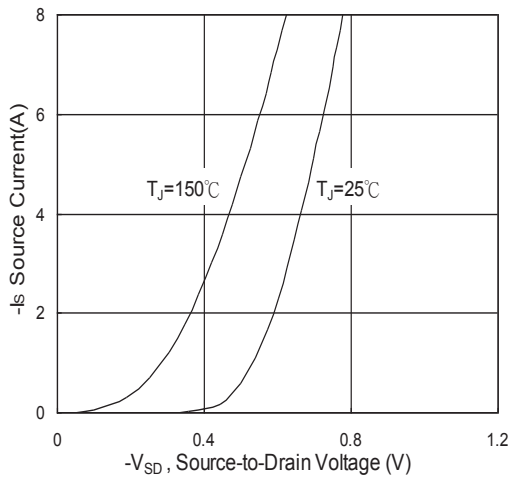


Fig.3 Forward Characteristics Of Reverse

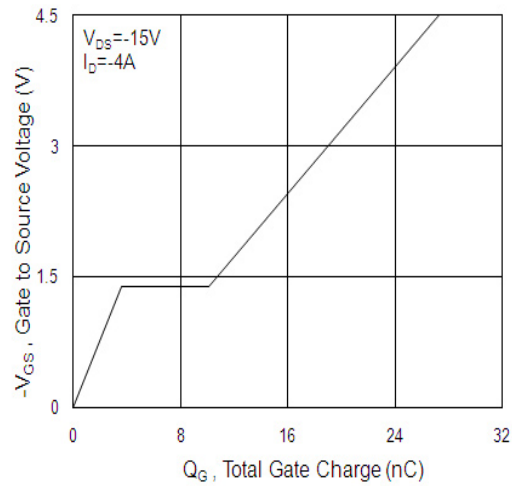


Fig.4 Gate-Charge Characteristics

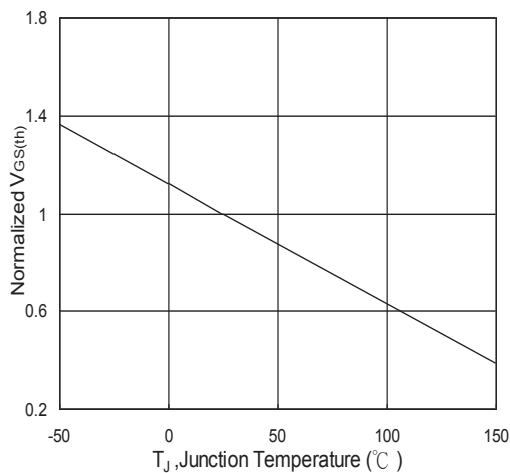


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

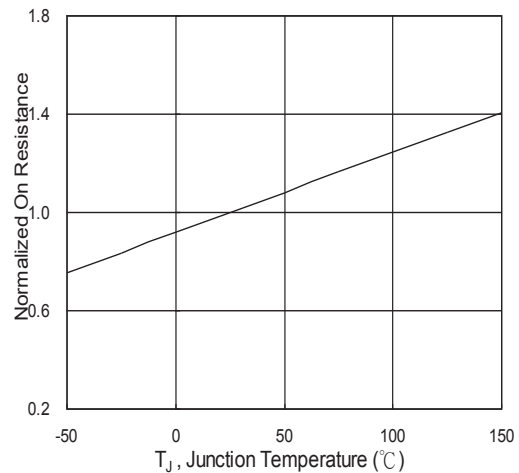


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

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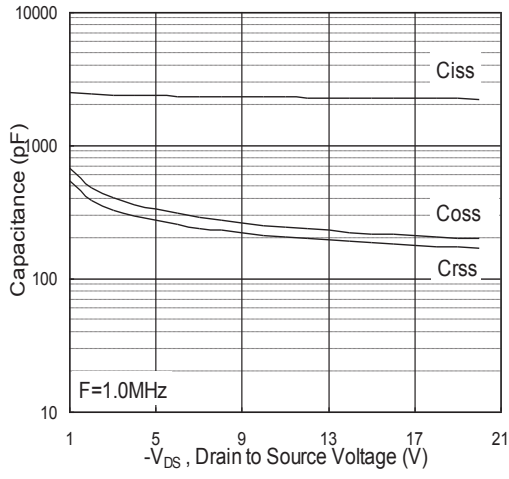


Fig.7 Capacitance

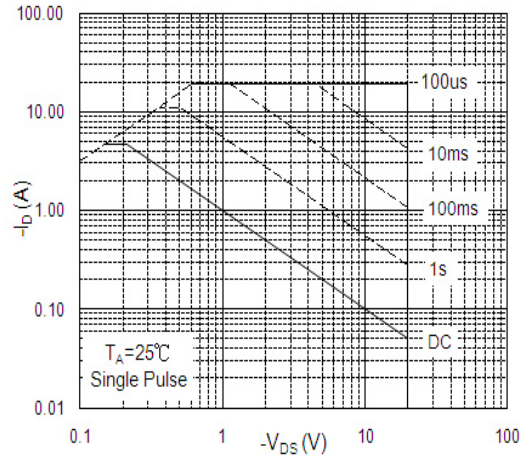


Fig.8 Safe Operating Area

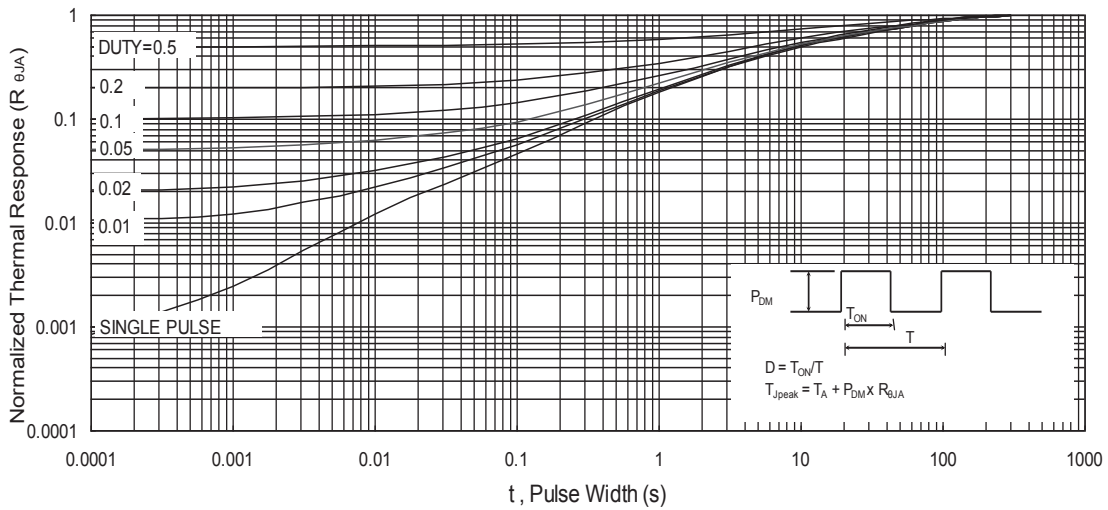


Fig.9 Normalized Maximum Transient Thermal Impedance

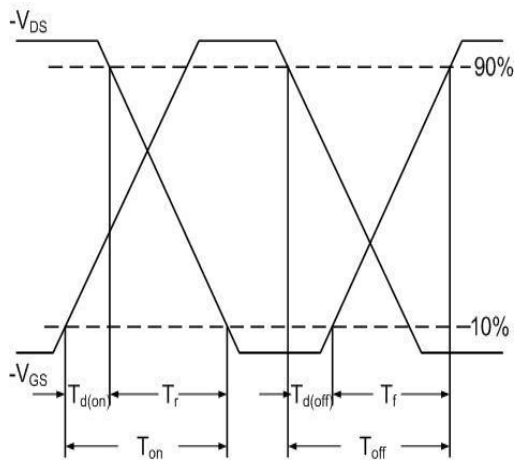


Fig.10 Switching Time Waveform

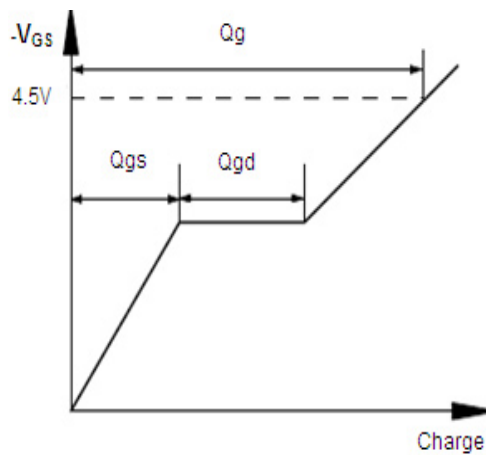


Fig.11 Gate Charge Waveform