ELM7C377142xA CMOS voltage detector, 2 channels, 18V operation, reset hold by ext.C

■General description

ELM7C377142xA is a 18V operation CMOS voltage detector for independent 2 lines power monitoring. It detects abnormalities such as power supply voltage interruptions or drops, and generates a reset signal. In addition to the 5V power supply line, VSB input can work for the another power supply line detection, and a reset signal is holded some period determined by an exterral capacitor.

■Features

- Detection voltages with hysteresis function.
- A reference voltage output capability.
- Minimal external parts(one capacitor).
- Over voltage detection.
- Accurate voltage detection : 4.2V±2.5%
- Detection voltage adjustable with 2 external resistors : 1.180V±1.5%
- Monitoring of two power supply lines : +5V and an arbitrary voltage
- Low voltage reset signal holding : Typ.0.8V
- Low power dissipation : Typ.65μA(Vcc=5V)
- Package : SOP-8 150mil
  SOP-8 208mil
  SON8-3×3

■Application

- Reset for Microprocessor, etc.

■Maximum absolute ratings

Parameter	Symbol	Limit	Unit
Power supply	Vcc	20	V
Input Voltage	Vsa	Vss-0.3 to Vcc+0.3 (<+8.0)	V
	Vsb	Vss-0.3 to +8.0	
	Vsc		
$\overline{\text{RESET}}$ output Voltage	Voh	Vss-0.3 to Vcc+0.3 (<+5.5)	V
OUTC output Voltage		Vss-0.3 to +5.5	
Power dissipation	Pd	680 (SOP-8 150mil) *1	mW
		680 (SOP-8 208mil) *1	
		600 (SON8-3×3) * 2	
Operating temperature	Top	-40 to +85	℃
Storage temperature	Tstg	-55 to +150	℃

* 1) When mounted on glass epoxy substrate with single layer FR4 70mm x 70mm x 1.6mm.
2) When mounted on 114.3mmx76.2mmx1.57mm 's two-layer FR4 glass epoxy board (based on EIA / JESD51-3/-5/-7).

■Selection guide

ELM7C377142xA-x

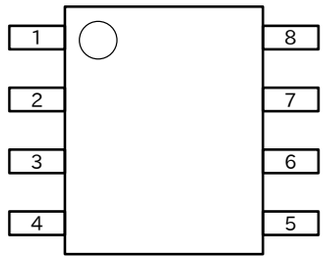
Symbol		
a, b	Detection voltage	42: Vsal=4.2V
c	Package	D: SOP-8 150mil P: SOP-8 208mil G: SON8-3×3
d	Product version	A
e	Taping direction	S: SON8-3×3 (Refer to PKG file) N: SOP-8 (Refer to PKG file)

* Taping direction is one way.

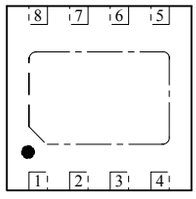
ELM7C3771 4 2 x A - x
↑ ↑ ↑ ↑ ↑
a b c d e

■Pin configuration

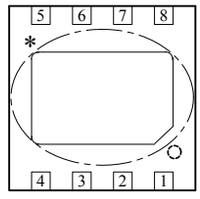
SOP-8(TOP VIEW)



SON8-3x3(TOP VIEW)



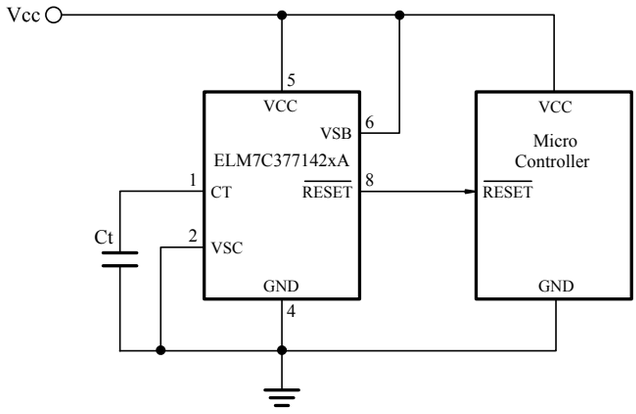
SON8-3x3(BOTTOM VIEW)



* The potential of the tab on the back is the ground(GND) level.
Please connect to GND pin(recommended) or set it to be open.

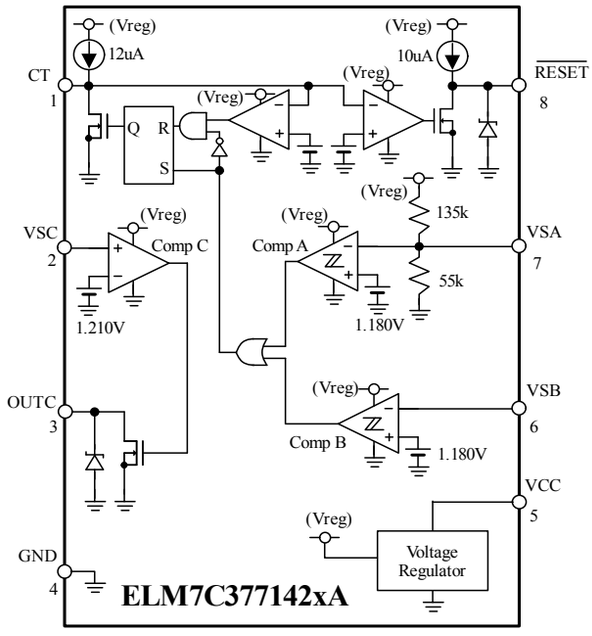
Pin No.	Pin name	Description
1	CT	Power-on reset hold time setting capacitor connection pin
2	VSC	Comparator C plus input pin
3	OUTC	Comparator C inverted output pin
4	GND	Ground pin
5	VCC	Power supply pin
6	VSB	Comparator B minus input pin
7	VSA	Comparator A minus input pin
8	$\overline{\text{RESET}}$	Outputs reset pin (negative logic)

■Standard circuit



* The OUTC of pin3 and the VSA of pin7 are open.
* Please be careful that the input voltage of the VSB of pin6 does not exceed the maximum absolute ratings. It is recommended that the input voltage at the VSB pin be less or equal than 6.5V.

■Block diagram



■Functional descriptions

Comparators Comp.A and Comp.B apply a hysteresis to the detected voltage, so that when the voltage at either the Vsa or Vsb pin falls below 1.180V the $\overline{\text{RESET}}$ output signal goes to “low” level.

Comp.B may be used to detect any given voltage(Application Circuit 3 : Arbitrary Voltage Supply Monitor), and can also be used as a forced reset pin (with reset hold time) with TTL input (Application Circuit 6 : 5V Power Supply Monitor with forced RESET input (Vcc=5V)). Note that if Comp.B is not used, the Vsb pin should be connected to the Vcc pin (Application Circuit 1 : 5V Power Supply Monitor). Here, please be careful that the input voltage of the VSB pin does not exceed the maximum absolute ratings. It is recommended that the input voltage at the VSB pin be less or equal than 6.5V.

Instantaneous breaks or drops in the power supply can be detected as abnormal conditions by the ELM7C377142xA within a 2μs interval.However because momentary breaks or drops of this duration do not cause problems in actual systems in some cases, a delayed trigger function can be created by connecting capacitors to the Vsa or Vsb pin (Application Circuit 9 : Supply Voltage Monitoring with Delayed Trigger).

Because the $\overline{\text{RESET}}$ output has built-in pull-up resistance, there is no need to connect to external pull-up resistance when connected to a high impedance load such as a CMOS logic IC.

Comparator Comp.C is an open-drain output comparator without hysteresis, in which the polarity of input/output characteristics is reversed. Thus Comp.C is useful for positive logic RESET signal output (Application Circuit 8 : 5V Power Supply Monitor with Non-inverted RESET), as well as for creating a reference voltage (Application Circuit 7 : 1.210V Reference voltage generation and 5V monitoring). Note that if Comp. C is not used, the Vsc pin should be connected to the GND pin (Application Circuit 1 : 5V Power Supply Monitor).

When VCC exceeds approximately 5.7 V, the internal circuit is regulated to this voltage.

Also, 5.7 V Zener diodes are built in at the output terminal and input terminal to protect the circuit.

Therefore, when VCC is 5.7 V or more, the H output level of $\overline{\text{RESET}}$ output terminal and OUTC output terminal is 5.7 V instead of applied VCC level.

■Electrical characteristics

Vcc=5.0V, Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	-	1.2	5.0	18.0	V
Power supply current	Icc1	Vsb=5.0V, Vsc=0.0V	-	65	(130)	µA
	Icc2	Vsb=0.0V, Vsc=0.0V	-	75	(150)	
Detection voltage	Vsal	Vcc falling	4.10	4.20	4.30	V
		Top=-40°C to +85°C	(4.05)*	4.20	(4.35)*	
	Vsah	Vcc rising	4.20	4.30	4.40	V
		Top=-40°C to +85°C	(4.15)*	4.30	(4.45)*	
Hysteresis width	Vhysa	Vsah-Vsal	50	100	150	mV
Detection voltage	Vsb	Vsb falling	1.162	1.180	1.198	V
		Top=-40°C to +85°C	(1.152)*	1.180	(1.208)*	
Deviation of detection voltage	ΔVsb	Vcc=3.5V to 6.0V	-	3	10	mV
Hysteresis width	Vhysb	-	15	30	45	mV
Input current	Iihb	Vsb=5.0V		0	0.25	µA
	Iilb	Vsb=0.0V	-0.25	0	-	
Output voltage	Vohr	I$\overline{\text{reset}}$=-5µA, Vsb=5.0V	4.50	4.90	-	V
	Volr	I$\overline{\text{reset}}$=3mA, Vsa=0.0V	-	0.28	0.40	
		I$\overline{\text{reset}}$=10mA, Vsa=0.0V	-	0.38	0.50	
Output sink current	I$\overline{\text{reset}}$	Volr=1.0V, Vsa=0.0V	20	60		mA
Ct charge current	Ict	Vsb=5.0V, Vct=0.5V	9	12	16	µA
Input current	Iihc	Vsc=5.0V	-	0	0.5	µA
	Iilc	Vsc=0.0V	-0.5	0	-	
Detection voltage	Vsc	-	1.192	1.210	1.228	V
		Top=-40°C to +85°C	(1.181)*	1.210	(1.239)*	
Deviation of detection voltage	ΔVsc	Vcc=3.5V to 6.0V	-	3	10	mV
Output leakage current	Iohc	Vohc=5.0V	-	0	1.0	µA
Output voltage	Volc	Ioutc=4mA, Vsc=5.0V	-	0.15	0.40	V
Output sink current	Ioutc	Volc=1.0V, Vsc=5.0V	6	15	-	mA
$\overline{\text{RESET}}$ signal holding minimum supply voltage	Vccl	Volr=0.4V, I$\overline{\text{reset}}$=200µA	-	0.8	1.2	V
Vsa, Vsb input pulse width	tpi	-	5.0	-	-	us
Reset hold time	tpo	Ct=0.01µF	0.5	1.0	1.5	ms
$\overline{\text{RESET}}$ rise time	tr	Rl=2.2kΩ, Cl=100pF	-	1.0	1.5	us
$\overline{\text{RESET}}$ fall time	tf		-	0.1	0.5	us
Propagation delay time	tpd	VSB pin	-	2	10	us
	tphl	VSC pin, Rl=2.2kΩ, Cl=100pF	-	0.5	-	us
	tplh		-	1.0	-	us

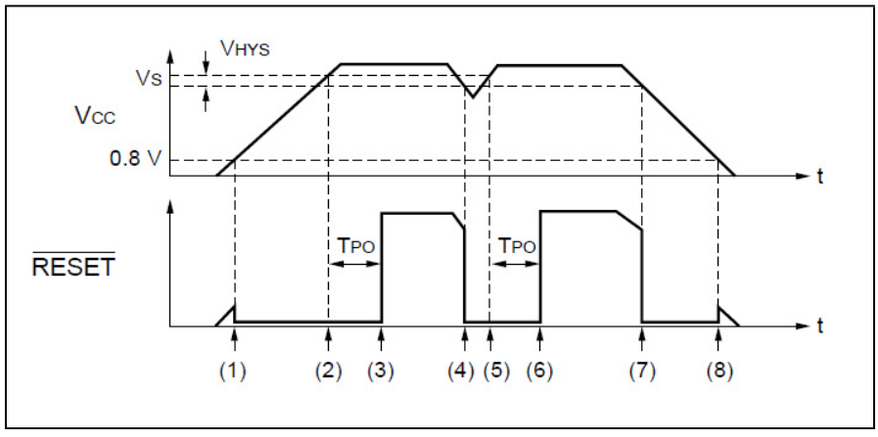
* The values enclosed in parentheses ( ) are setting assurance values.

* Ct range is 0.001 µF to 10 µF.

* The voltage range is 10% to 90% at testing the reset output transition time.

■Timing chart

Fig.1: Basic operation

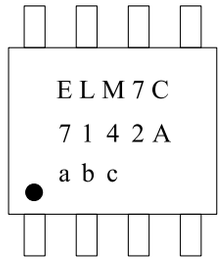


■Function Explanation

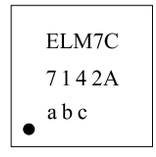
(1) When Vcc rises to about 0.8 V, $\overline{\text{RESET}}$ goes Low.
(2) When Vcc reaches Vs +Vhys, Ct then begins charging. $\overline{\text{RESET}}$ remains low during this time.
(3) $\overline{\text{RESET}}$ goes high after a certain period Tpo.
Tpo ≈ Ct × 10^5 (Refer to "Reset hold time(tpo) vs. Ct pin capacitance" in "■Typical characteristic curves.")
(4) When Vcc level drops lower then Vs, then $\overline{\text{RESET}}$ goes low and Ct starts discharging.
(5) When Vcc level reaches Vs + Vhys, then Ct starts charging.In the case of voltage sagging, if the period from the time Vcc goes lower than or equal to Vs to the time Vcc reaches Vs +Vhys again, is longer than tpi, Ct is discharged and charged successively.
(6) After Tpo passes, and Vcc level exceeds Vs + Vhys, then $\overline{\text{RESET}}$ goes high.
(7) When Vcc becomes less than Vs, (4) to (6) is repeated.
(8) If Vcc drops to 0V, $\overline{\text{RESET}}$ keeps "Low" until Vcc reaches 0.8V.

■Marking

SOP-8



SON8-3×3

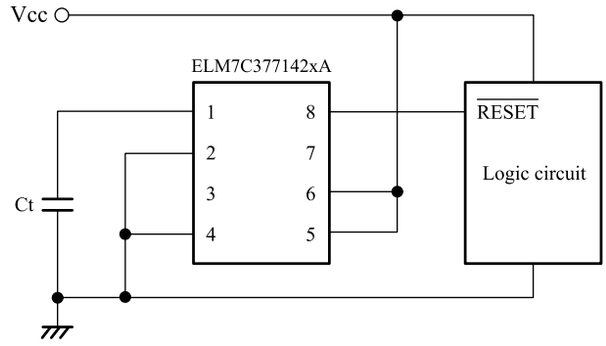


Symbol	Mark	Content
a	0 to 9	Last numeral of A.D.
b	A to M (excepted I.)	Assembly month
c	0 to 9	Lot No.

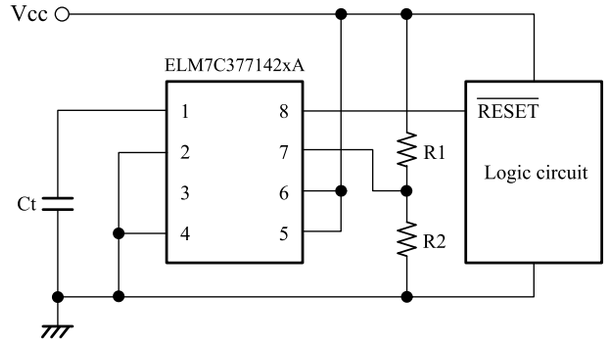
■Application circuit example

1) 5V Power Supply Monitor

Monitored by Vsa. Detection threshold voltage is Vsal and Vsah.



2) 5V Power Supply Voltage Monitor (Externally Fine-Tuned Type)



The Vsa detection voltage can be adjusted externally.

Resistance R1 and R2 are set sufficiently lower than the IC internal partial voltage resistance, so that the detection voltage can be set using the ratio between resistance R1 and R2. (Refer to the table below).

* R1, R2 calculation formula (when R1 << 100 kΩ, R2 <<40 kΩ)

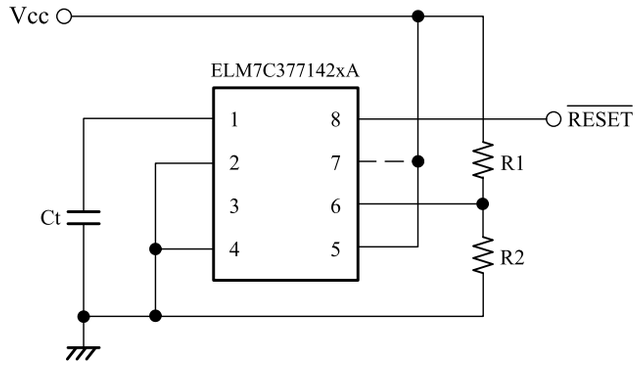
Vsal≈(R1+R2)×1.18/R2[V], Vsah≈(R1+R2)×1.21/R2[V]

R1(kΩ)	R2(kΩ)	Detection voltage : Vsal(V)	Detection voltage : Vsah(V)
10.00	3.90	4.21	4.31
9.10	3.90	3.93	4.03

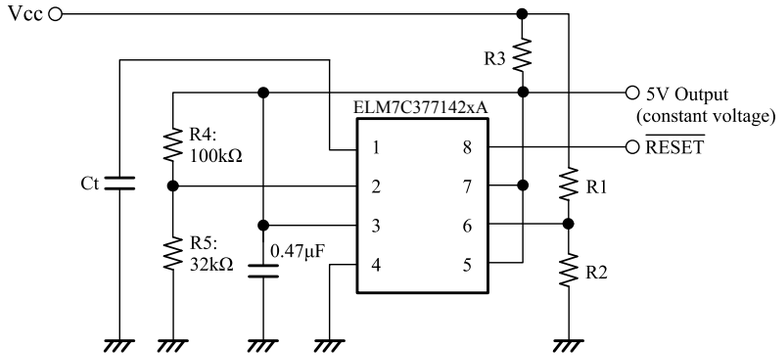
3) Arbitrary Voltage Supply Monitor-1 (Vcc≤5.5V)

* Detection Voltage can be set by R1 and R2. Detection Voltage = (R1 + R2) × 1.18/R2
* Connect Pin7 to Vcc when Vcc less than 4.45V.
* Pin7 can be opened when Vcc greater than 4.45V. Power dissipation can be reduced. Consumption current decreases when pin7 is open.

Note: Hysteresis of 30mV at Vsb at termination is available. Hysteresis width dose not depend on (R1+R2).



4) Arbitrary Voltage Supply Monitor-2 (Vcc>5.5V)

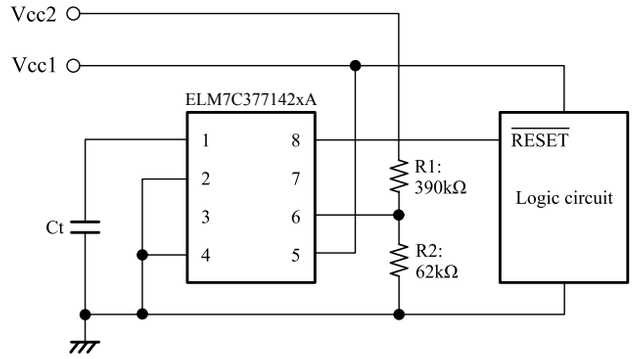


* Detection Voltage can be set by R1 and R2. Detection Voltage=(R1 + R2) × 1.18/R2
* The $\overline{\text{RESET}}$ signal output is ≈ 0V(low level) and ≈ 5V(high level). Vcc voltage cannot be output. Do not pull up $\overline{\text{RESET}}$ to Vcc.
* Changing the resistance ratio between R4 and R5 changes the constant voltage output, thereby changing the voltage of the high level $\overline{\text{RESET}}$ output. Note that the constant voltage output should not exceed 5.5V.
* The 5V output can be used as a power supply for control circuits with low current consumption.
* As an example of R3 value, R3 = (Vcc-5) /0.01 for 10mA output.

5) 5V and 12V Power supply monitor (2 types of power supply monitor Vcc1=5V, Vcc2 =12V)

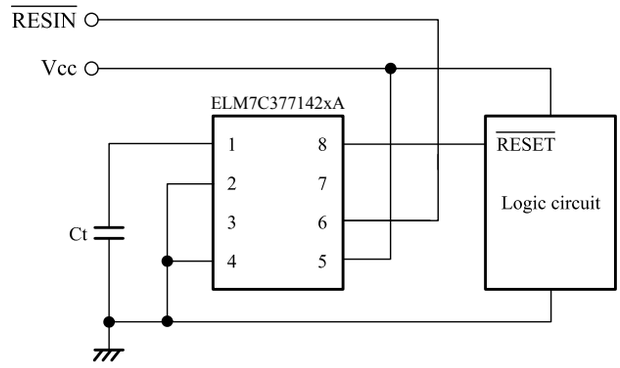
* 5V is monitored by Vsa. Detection voltage is about 4.2V.
* 12V is monitored by Vsb. When R1=390kΩ and R2=62kΩ, detection voltage is about 8.6V. Generally the detection voltage is determined by the following equation.

  Detection Voltage=(R1+R2)×1.18/R2



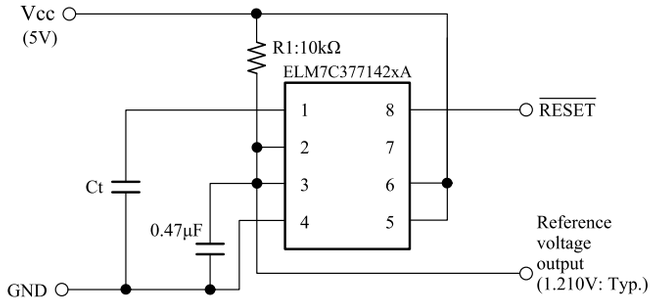
6) 5V Power supply monitor with forced RESET input (Vcc=5V)

$\overline{\text{RESIN}}$ is an TTL compatible input.



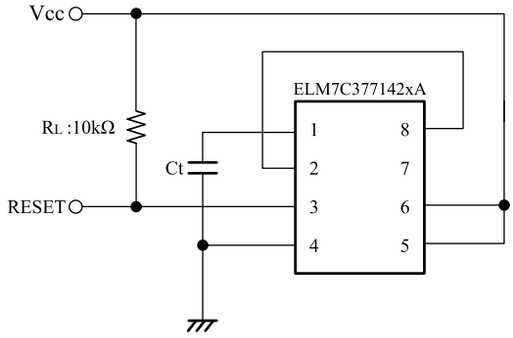
7) 1.210V Reference voltage generation and 5V monitoring

Resistor R1 determines Reference current. Using 1.2 kΩ as R1, reference current is about 2 mA.



8) 5V Power supply monitor with non-inverted $\overline{\text{RESET}}$

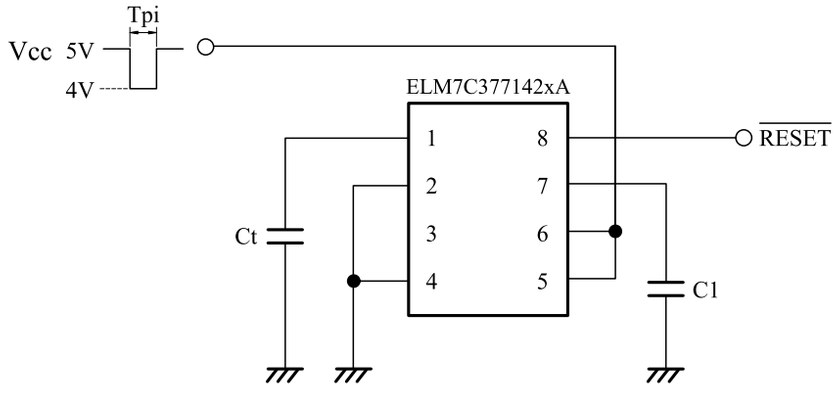
In this case, Comparator C is used to invert $\overline{\text{RESET}}$ signal. OUTC is an open-drain output. RL is used as a pull-up resistor. Here, please be careful that the input voltage of the VSB pin does not exceed the maximum absolute ratings. It is recommended that the input voltage at the VSB pin be less or equal than 6.5V.



9) Supply voltage monitoring with delayed trigger

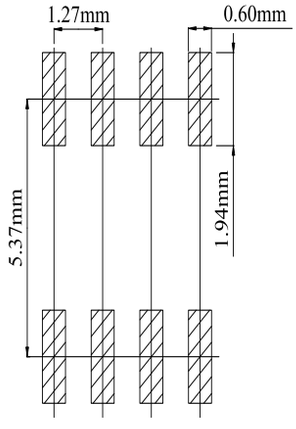
When the voltage shown in the diagram below is applied at Vcc, the minimum value of the input pulse width is increased to approximately 75µs (when C1=1000pF). The formula for calculating the minimum value of the input pulse width [Tpi] is : Tpi[µs]≈$7.5\times10^{-2}\times$C1[pF]

Here, please be careful that the input voltage of the VSB pin does not exceed the maximum absolute ratings. It is recommended that the input voltage at the VSB pin be less or equal than 6.5V.

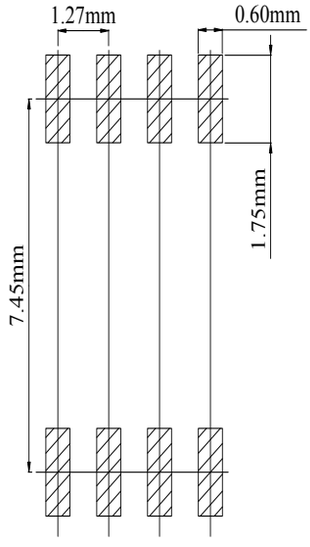


■Reference land pattern

SOP-8 150mil

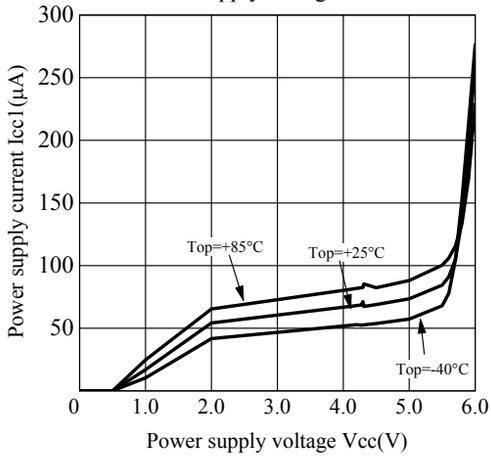


SOP-8 208mil

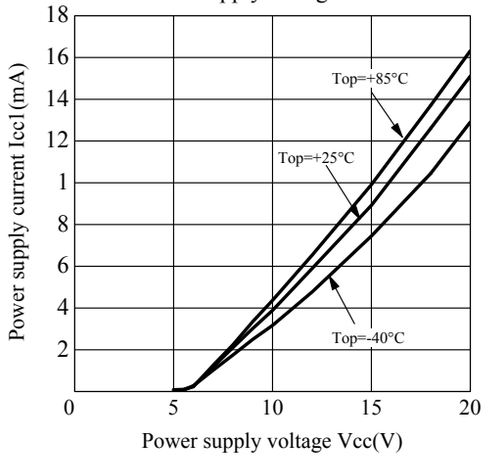


■Typical characteristic curves

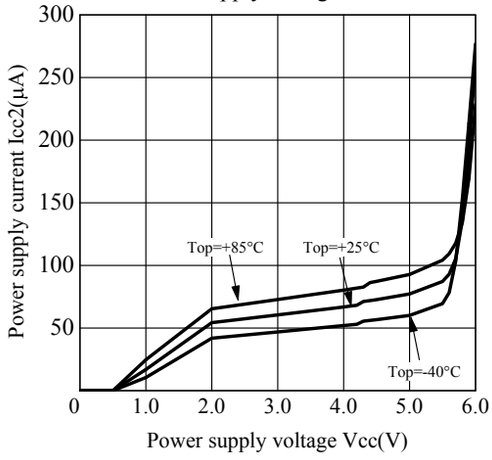
Power supply current (Icc1) vs.
Power supply voltage-1



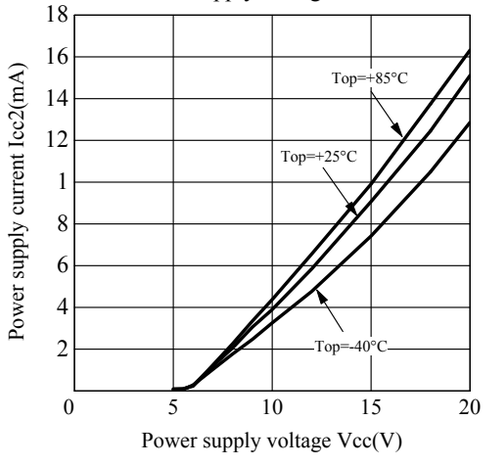
Power supply current (Icc1) vs.
Power supply voltage-2



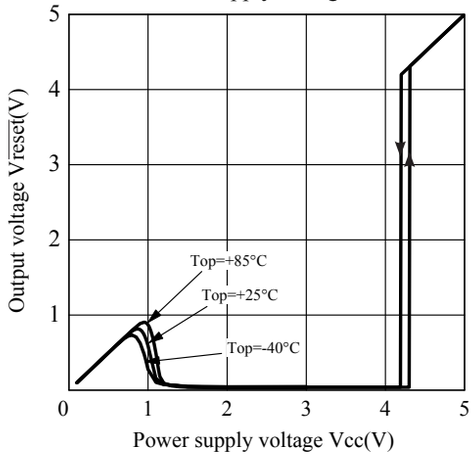
Power supply current (Icc2) vs.
Power supply voltage-1



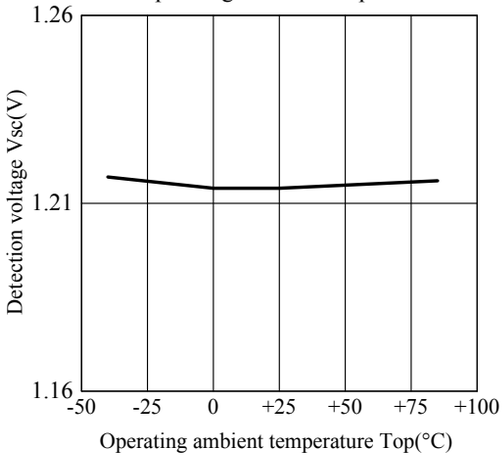
Power supply current (Icc2) vs.
Power supply voltage-2



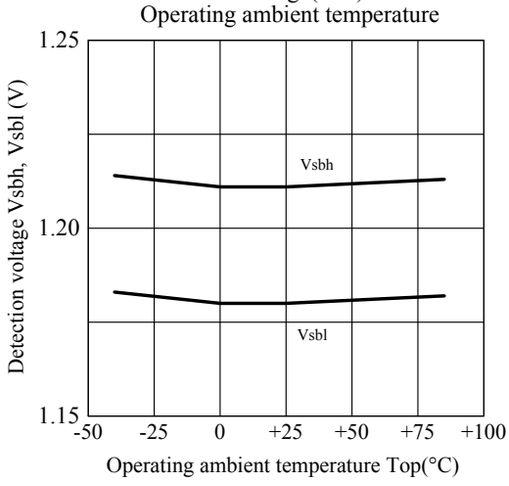
Output voltage ($\overline{\text{RESET}}$) vs.
Power supply voltage



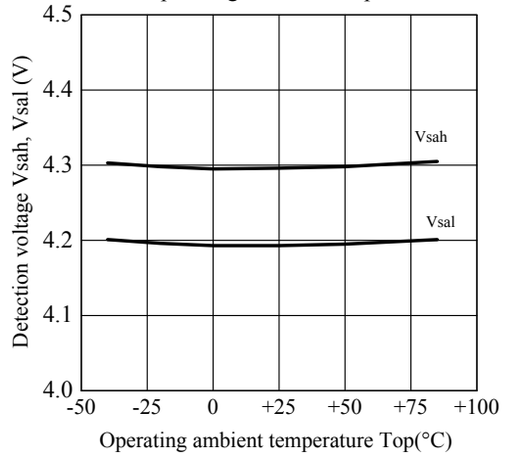
Detection voltage(Vsc) vs.
Operating ambient temperature



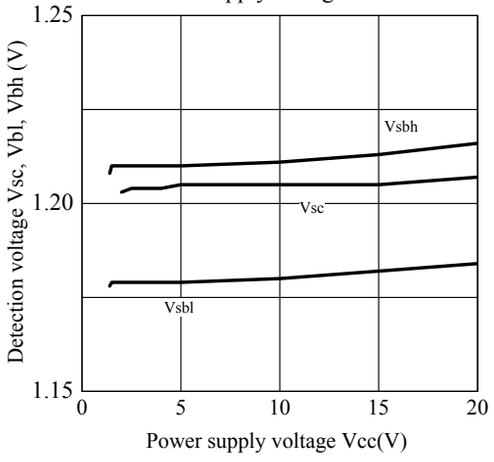
Detection voltage(Vsb) vs.
Operating ambient temperature



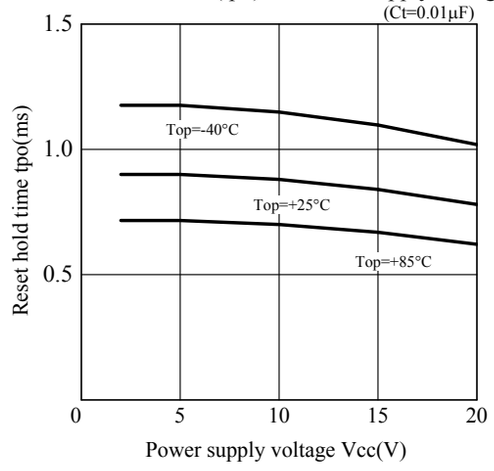
Detection voltage(Vsa) vs.
Operating ambient temperature



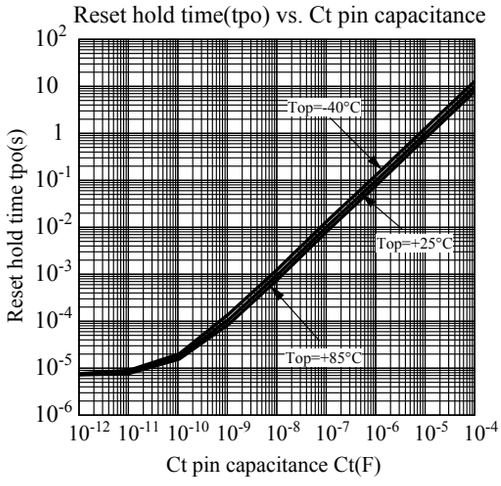
Detection voltage(Vsb,Vsc) vs.
Power supply voltage



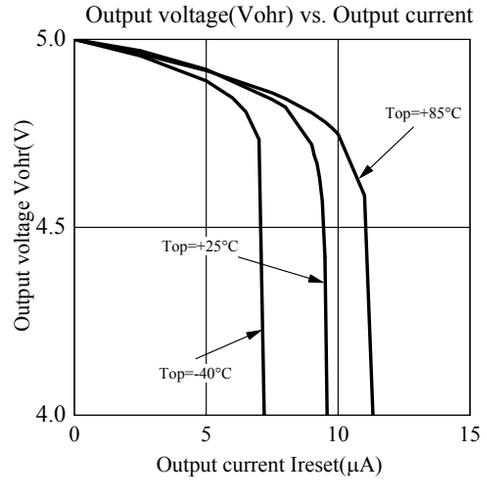
Reset hold time(tpo) vs. Power supply voltage
(Ct=0.01µF)

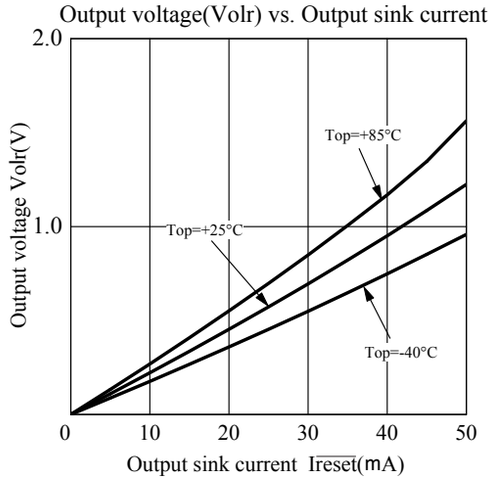


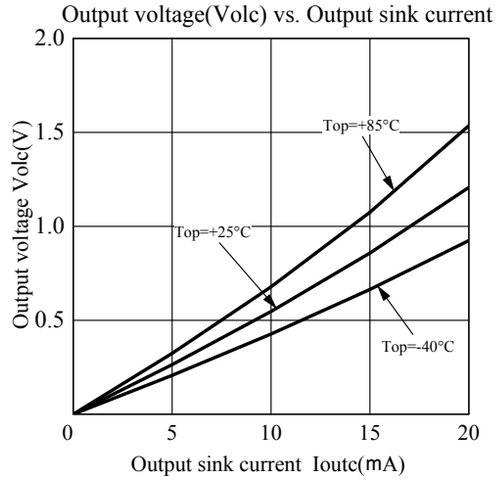
Reset hold time(tpo) vs. Ct pin capacitance



Output voltage(Vohr) vs. Output current




Output voltage(Volr) vs. Output sink current
2.0
1.0
Output voltage Volr(V)
Top=+85°C
Top=+25°C
Top=-40°C
0
10
20
30
40
50
Output sink current Ireset(mA)


Output voltage(Volc) vs. Output sink current
2.0
1.5
1.0
0.5
Output voltage Volc(V)
Top=+85°C
Top=+25°C
Top=-40°C
0
5
10
15
20
Output sink current Ioutc(mA)