ELM7C377342xA CMOS Voltage detector with watchdog timer

■General description

ELM7C377342xA is Power supply monitoring IC that instantaneously detects abnormalities such as instantaneous interruption or drop of power supply voltage and generates a reset signal. Since the watchdog timer is built in, various microcomputer systems can have a fail-safe function. It has output of both logic of RESET_B and RESET output with internal pull-up. In addition, the reference amplifier outputs the correct reference voltage externally.

■Features

- Detection voltage with hysteresis function.
- Watchdog timer by edge trigger input built in.
- Minimal external parts(one capacitor).
- Reset signal of both positive and negative logic outputs.
- Detect accurate supply voltage drop : 4.2V±2.5%
- Accurate reference voltage output : 1.245V±1.45%
- Low reset minimal power supply voltage : Typ.0.8V
- Package : SOP-8 150mil, SOP-8 208mil
  SON8-3×3

■Application

- Reset for Microprocessor, etc.

■Maximum absolute ratings

Parameter	Symbol	Limit	Unit
Power supply	Vcc	6.5	V
Input Voltage	Vs	Vss-0.3 to Vcc+0.3	V
	Vck		
RESET_B, RESET output Voltage	Voh	Vss-0.3 to Vcc+0.3	V
Power dissipation	Pd	300 (SOP-8)	mW
		500 (SON8-3×3)	
Operating temperature	Top	-40 to +85	°C
Storage temperature	Tstg	-55 to +125	°C

■Selection guide

ELM7C377342xA-x

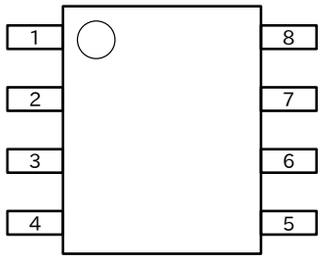
Symbol		
a, b	Detection voltage	42: Vsl=4.2V
c	Package	D: SOP-8 150mil P: SOP-8 208mil G: SON8-3×3
d	Product version	A
e	Taping direction	S: SON8-3×3 (Refer to PKG file) N: SOP-8 (Refer to PKG file)

* Taping direction is one way.

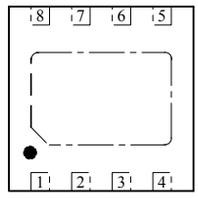
ELM7C3773 4 2 x A - x
↑ ↑ ↑ ↑ ↑
a b c d e

■Pin configuration

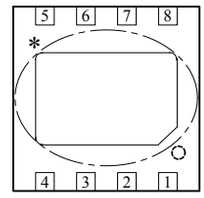
SOP-8(TOP VIEW)



SON8-3x3(TOP VIEW)



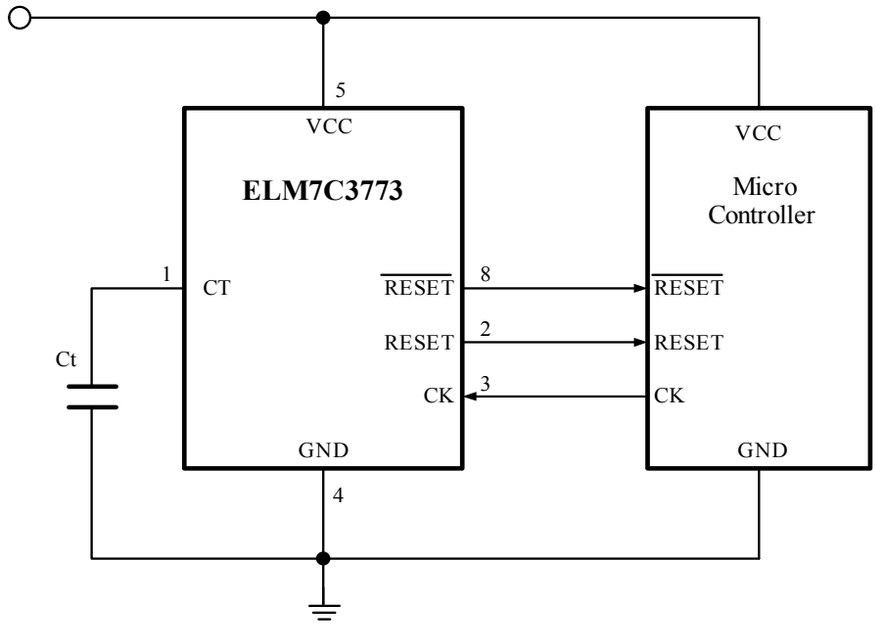
SON8-3x3(BOTTOM VIEW)



* The potential of the tab on the back is the ground(GND) level.
Please connect to GND pin(recommended) or set it to be open.

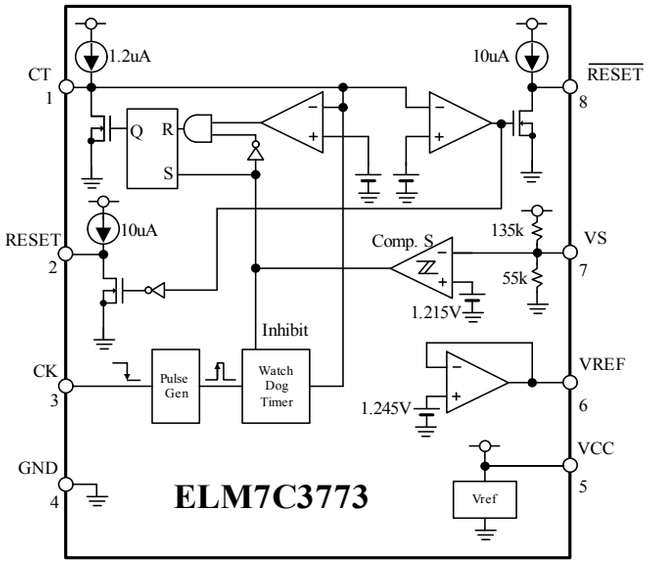
Pin No.	Pin name	Description
1	CT	Power-on reset hold time setting and Watchdog timer monitor time setting pin
2	RESET	Outputs reset pin (positive logic)
3	CK	Inputs clock pin
4	GND	Ground pin
5	VCC	Power supply pin
6	VREF	Reference voltage output pin
7	VS	Comparator minus input pin
8	$\overline{\text{RESET}}$	Outputs reset pin (negative logic)

■Standard circuit



* The VREF of pin6 and the VS of pin7 are open.

■Block diagram



■Functional descriptions

1. Comp.S

Comp.S is comparator including hysteresis. it compare the reference voltage and the voltage of Vs, so that when the voltage of Vs terminal falls below approximately 1.215V, reset signal outputs.

Instantaneous breaks or drops in the power can be detected as abnormal conditions by the ELM7C3773 within a 2 μs interval. However because momentary breaks or drops of this duration do not cause problems in actual systems in some cases, a delayed trigger function can be created by connecting capacitors to the Vs terminal.

2. Output circuit

A comparator is built in for turning on/off the $\overline{\text{RESET}}$/RESET outputs and, compare the voltage of the Ct terminal and the threshold voltage. Because the $\overline{\text{RESET}}$/RESET outputs have built-in pull-up circuit, there is no need to connect to external pull-up resistor when connected to a high impedance load such as CMOS logic IC.(It corresponds to 500 kΩ at Vcc = 5V.)

3. Pulse generation circuit

When the voltage of the CK terminal changes from the “high” level into the “Low” level, pulse generator is sent to the watch-dog timer by generating the pulse momentarily at the time of drop from the threshold level.

4. Watchdog timer circuit

When power-supply voltages fall more than detecting voltages, the watch-dog timer becomes an interdiction.

5. Reference amplifier

The Reference amplifier is an op-amp to output the reference voltage. If the comparator is put up outside, two or more power-supply voltage monitor and overvoltage monitor can be done.

6. Logic circuit

The logic circuit controls the charging and discharging of the power-on reset hold time setting and watch-dog timer monitor time setting capacitor(Ct).

■Electrical characteristics

Vcc=5.0V, Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	-	1.2	5.0	6.0	V
Supply current	Icc	Watch-dog timer operating	-	100	200	μA
Detection voltage	Vsl	Vcc falling	4.10	4.20	4.30	V
		Top=-40°C to +85°C	(4.05)*	4.20	(4.35)*	
	Vsh	Vcc rising	4.20	4.30	4.40	V
		Top=-40°C to +85°C	(4.15)*	4.30	(4.45)*	
Hysteresis width	Vshys	Vsh-Vsl	50	100	150	mV
Reference voltage	Vref	Vcc=3.5V to 6.0V	1.227	1.245	1.263	V
		Top=-40°C to +85°C	(1.215)*	1.245	(1.275)*	
Reference voltage change rate	ΔVref1	Vcc=3.5V to 6.0V	-	3	10	mV
Reference voltage outputloading change rate	ΔVref2	Iout=-200μA to +5μA	-5	-	5	mV
CK threshold voltage	Vth1	CK falling, Top=-40°C to +85°C	0.80	1.25	2.00	V
CK input current	Iih	Vih=5.0V	-	0	1.0	μA
	Iil	Vil=0.0V	-1.0	0	-	
Ct discharge current	Ictd	Watch-dog timer operating, Vct=1.0V	(8.5)	11.0	(14.5)	μA
High level output voltage	Voh1	Vs open, I$\overline{\text{reset}}$=-5μA	4.5	4.9	-	V
	Voh2	Vs=0.0V, Ireset=-5μA	4.5	4.9	-	
Output saturation voltage	Vol1	Vs=0.0V, I$\overline{\text{reset}}$=3mA	-	0.2	0.4	V
	Vol2	Vs=0.0V, I$\overline{\text{reset}}$=10mA	-	0.3	0.5	
	Vol3	Vs open, Ireset=3mA	-	0.2	0.4	
	Vol4	Vs open, Ireset=10mA	-	0.3	0.5	
Output sink current	Iol1	Vs=0.0V, V$\overline{\text{reset}}$=1.0V	20	60	-	mA
	Iol2	Vs open, Vreset=1.0V	20	60	-	
Ct charge current	Ictu	Power on reset operating, Vct=1.0V	(0.5)	1.2	(2.5)	μA
Min supply voltage for $\overline{\text{RESET}}$	Vccl1	V$\overline{\text{reset}}$=0.4V, I$\overline{\text{reset}}$=0.2mA	-	0.8	1.2	V
Min supply voltage for RESET	Vccl2	Vreset=Vcc-0.1V, RL=1MΩ(Between RESET and GND)	-	0.8	1.2	
Vcc input pulse width	tpi	Vcc : 5V → 4V → 5V	8.0	-	-	us
CK input pulse width	tckw	CK : Positive pulse or negative pulse	3.0	-	-	us
CK input frequency	tck	-	20	-	-	us
Watch-dog timer watching time	twd	Ct=0.1μF *	5	10	15	ms
Watch-dog timer reset time	twr	Ct=0.1μF	1	2	3	ms
Rising reset hold time	tpr	Ct=0.1μF, Vcc rising	50	100	150	ms
Output propagationdelay time from Vcc	tpd1	$\overline{\text{RESET}}$, RL=2.2kΩ, CL=100pF	-	2	10	us
	tpd2	RESET, RL=2.2kΩ, CL=100pF	-	3	10	
Output rising time*	tr	RL=2.2kΩ, CL=100pF	-	1.0	1.5	us
Output falling time*	tf		-	0.1	0.5	

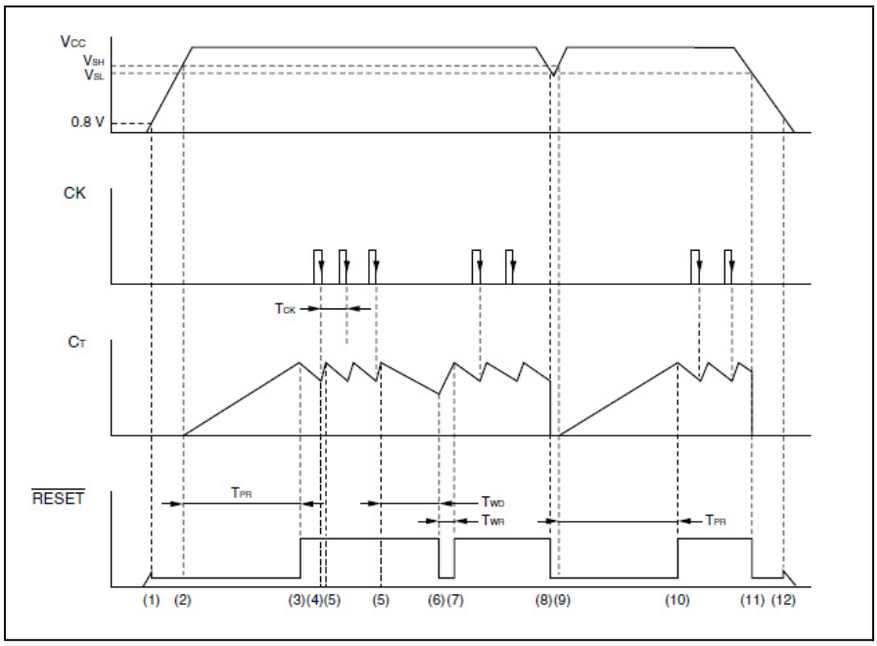
* The values enclosed in parentheses ( ) are setting assurance values.

* Ct range is 0.001 μF to 10 μF.

* The voltage range is 10% to 90% at testing the reset output transition time.

■Timing chart

Fig.1: Basic operation



■Operation sequence

(1) When Vcc rises to about 0.8V, $\overline{\text{RESET}}$ goes “Low” and RESET goes “High”. The pull-up current of approximately 1μA (Vcc = 0.8V) is output from RESET.

(2) When Vcc rises to VSH (≈ 4.3V), the charge with Ct starts.At this time, the output is being reset.

(3) When Ct has been charged for a certain period of time Tpr, RESET goes “High” and $\overline{\text{RESET}}$ goes “Low”.

Reset hold time: Tpr (ms) ≈ 1000 × Ct (μF)

After releasing reset, the discharge of Ct starts, and watch-dog timer operation starts. Tpr is not influenced by the CK input.

(4) C changes from the discharge into the charge if the clock (Negative edge) is input to the CK terminal while discharging Ct.

(5) Ct changes from the charge into the discharge when the voltage of CT reaches a constant threshold (≈ 1.245 V). (4) and (5) are repeated while a normal clock is input by the logic system.

(6) When the clock is cut off, and the voltage of Ct falls on threshold (≈ 0.35V) of reset on, $\overline{\text{RESET}}$ goes “Low” and RESET goes “High”.Discharge time of CT until reset is output: Twd is watch-dog timer monitoring time.

Twd (ms) ≈ 100 × Ct (μF)

Because the charging time of Ct is added at accurate time from stop of the clock and getting to the output of reset of the clock, Twd becomes maximum Twd + Twr by minimum Twd.

(7) Reset time in operating watch-dog timer : Twr is charging time where the voltage of Ct goes up to off threshold (≈ 1.245V) for reset.

twr (ms) ≈ 20 × Ct (μF)

Reset of the output is released after Ct reaches an off threshold for reset, and Ct starts the discharge, after that if the clock is normally input, operation repeats (4) and (5), when the clock is cut off, operation repeats (6) and (7).

(8) When Vcc falls on Vsl (≈ 4.2V), reset is output. Ct is rapidly discharged at the same time.

(9) When Vcc goes up to Vsh, the charge with Ct is started. When Vcc is momentarily low, After falling Vsl or less Vcc, the time to going up is the standard value of the Vcc input pulse width in Vsh or more. After the charge of Ct is discharged, the charge is started if it is Tpi or more.

(10) Reset of the output is released after Tpr, after Vcc becomes Vsh or more, and the watch-dog timer starts. After that, when Vcc becomes Vsl or less, (8) to (10) is repeated.

(11) While power supply is off, when Vcc becomes Vsl or less, reset is output.

(12) The reset output is maintained until Vcc becomes 0.8V when Vcc falls on 0V.

(13) Equation of the time setting capacity Ct and each setting time:

tpr(ms) ≈ 1000 × Ct(μF)

twd(ms) ≈ 100 × Ct(μF)

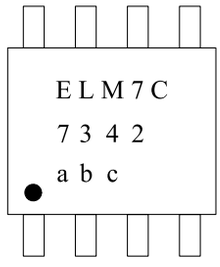
twr(ms) ≈ 20 × Ct(μF)

Example (When Ct = 0.1 μF)

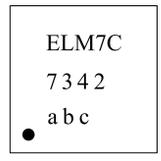
tpr [ms]	twd [ms]	twr [ms]
100	10	2

■Marking

SOP-8



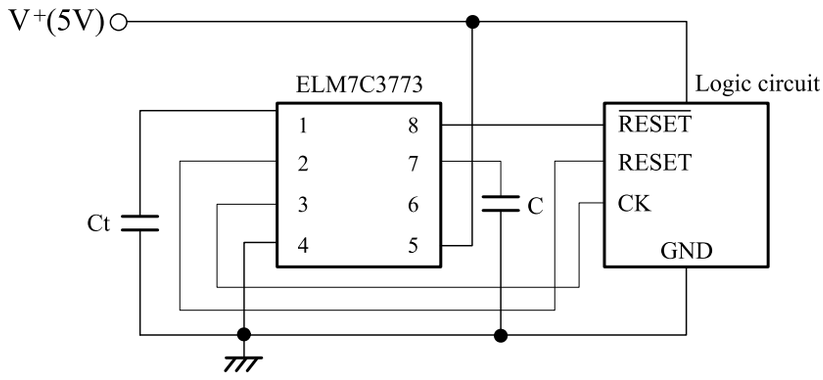
SON8-3×3



Symbol	Mark	Content
a	0 to 9	Last numeral of A.D.
b	A to M (excepted I.)	Assembly month
c	0 to 9	Lot No.

■Application circuit example

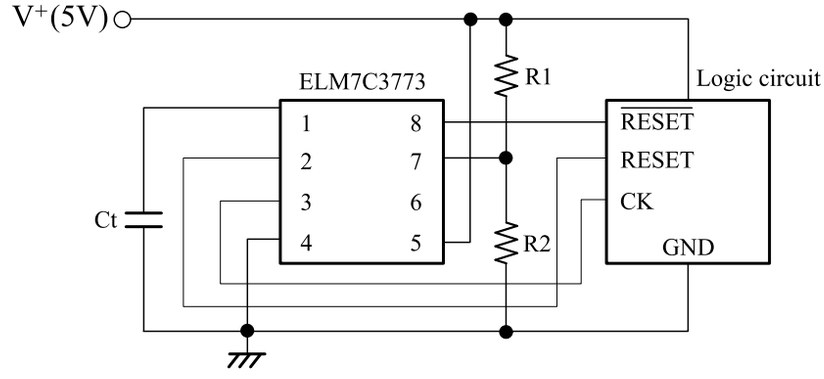
1) Monitoring 5V supply voltage and watchdog timer



∗ Supply voltage is monitored using Vs. Detection voltage are Vsh and Vsl.

∗ By adding an external capacitor C between the Vs terminal and GND, the minimum input pulse width Tpi can be lengthened.

2) 5V Supply Voltage Monitoring (external fine-tuning type)

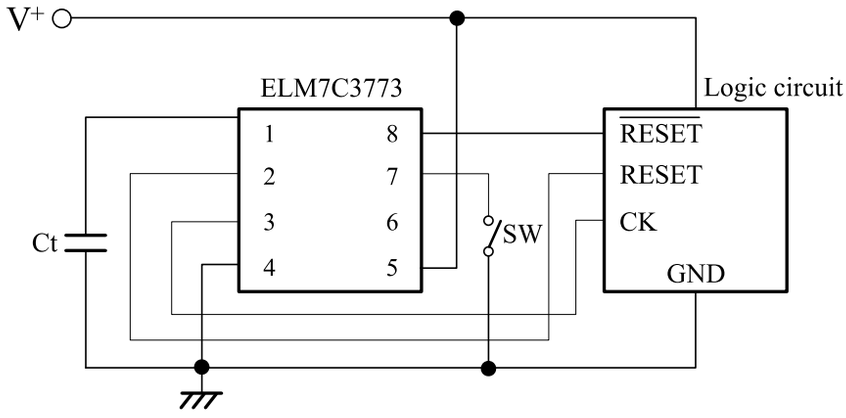


* Vs detection voltage can be adjusted externally.

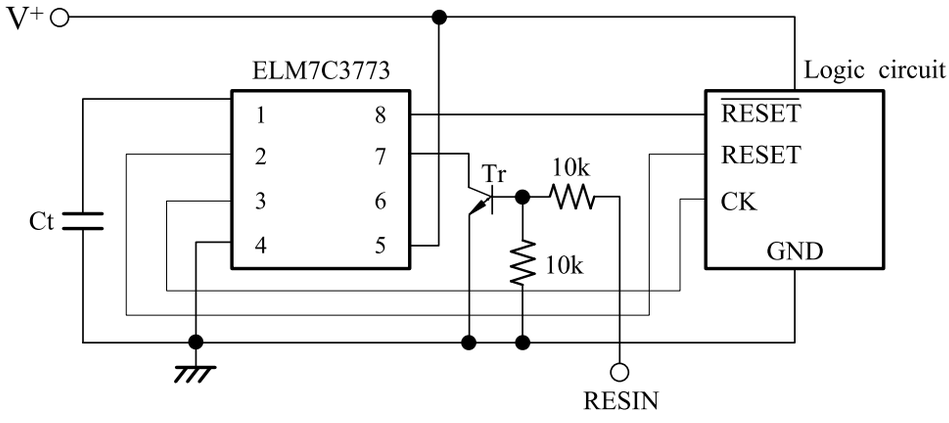
* Based on selecting R1 and R2 values that are sufficiently lower than the resistance of the IC's internal voltage divider, the detection voltage can be set according to the resistance ratio of R1 and R2 (Refer to the table below.)

R1(kΩ)	R2(kΩ)	Detection voltage: Vsl(V)	Detection voltage: Vsh(V)
10.0	3.9	4.32	4.43
9.1	3.9	4.06	4.16

3) With Forced Reset (with reset hold)



* Grounding pin 7 at the time of SW ON sets $\overline{\text{RESET}}$ (pin 8) to Low and RESET (pin 2) to High.



* Feeding the signal to terminal RESIN and turning on Tr sets the $\overline{\text{RESET}}$ terminal to Low and the RESET terminal to High.

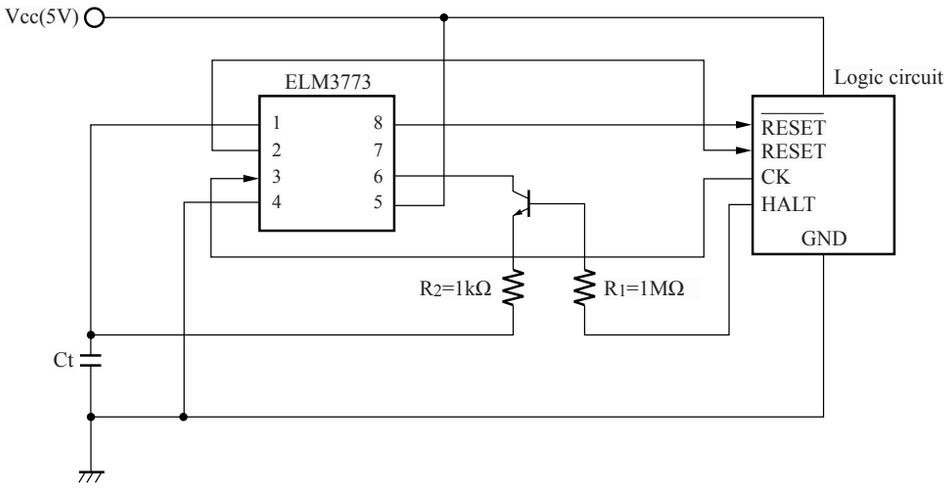
4) Stopping Watch-dog Timer (Monitoring only supply voltage)

These are example application circuits in which the ELM377342xA monitors supply voltage alone without resetting the microprocessor even if the latter, used in standby mode, stops sending the clock pulse to the ELM377342xA.

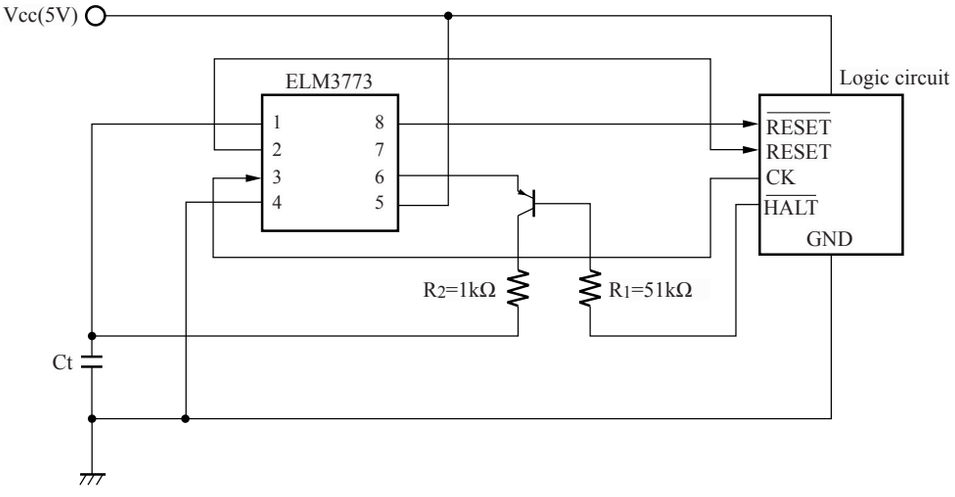
(Notes)

The watch-dog timer is inhibited by clamping the Ct terminal voltage to Vref. The supply voltage is constantly monitored even while the watch-dog timer is inhibited. For this reason, a reset signal is output at the occurrence of either instantaneous disruption or a sudden drop to low voltage. Note that in application examples (a) and (b), the hold signal is inactive when the watch-dog timer is inhibited at the time of resetting.If the hold signal is active when the microprocessor is reset, the solution is to add a gate, as in examples (c) and (d).

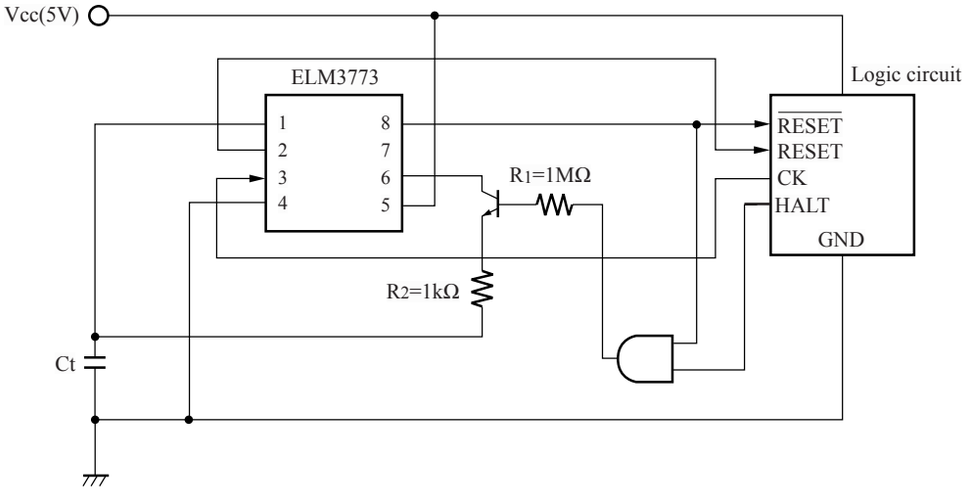
(a) Using NPN transistor



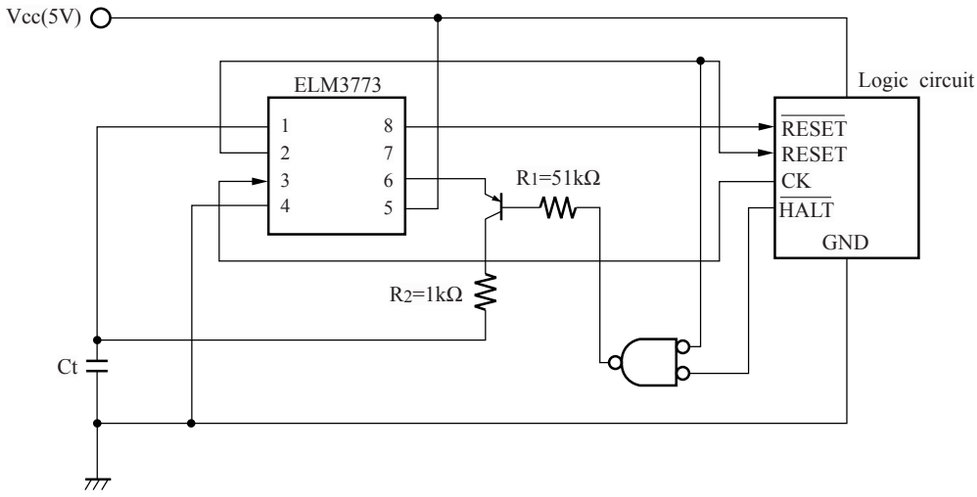
(b) Using PNP transistor



(c) Using NPN transistor

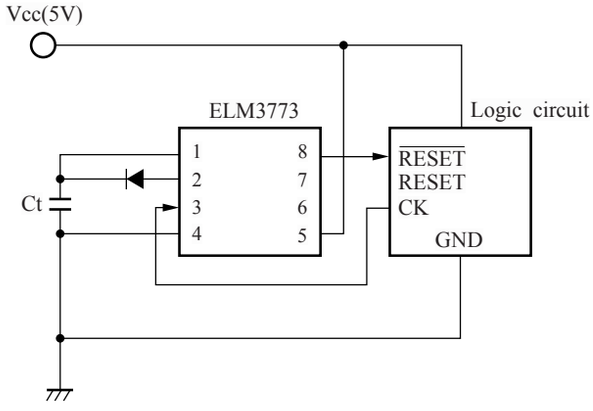


(d) Using PNP transistor

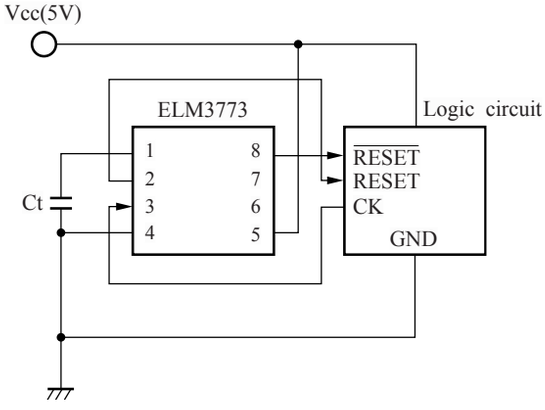


5) Reducing Reset Hold Time

(a) Tpr reduction method



(b) Standard usage



(Notes)

- $\overline{\text{RESET}}$ is the only output that can be used.
- Standard Tpr, Twd and Twr value can be found using the following formulas.

  <Formulas>

  Tpr (ms) ≈ 100×Ct (μF)

  Twd (ms) ≈ 100×Ct (μF)

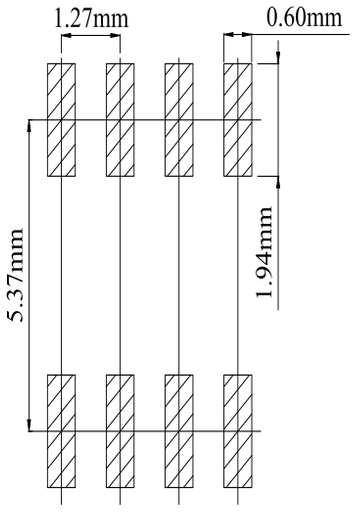
  Twr (ms) ≈ 16×Ct (μF)
- The above formulas become standard values in determining Tpr, Twd and Twr. Reset hold time is compared below between the reduction circuit and the standard circuit.

Ct = 0.1μF

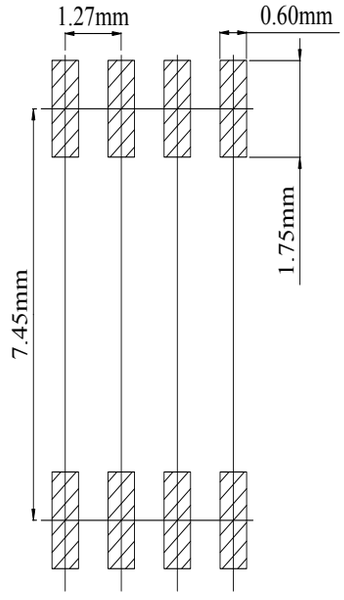
	Tpr reduction circuit	Standard circuit
Tpr ≈	10 ms	100 ms
Twd ≈	10 ms	10 ms
Twr ≈	1.6 ms	2.0 ms

■Reference land pattern

SOP-8 150mil

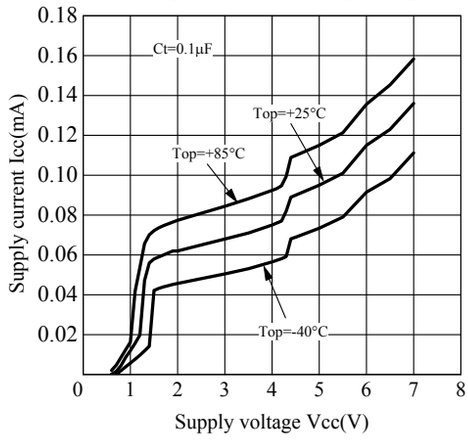


SOP-8 208mil

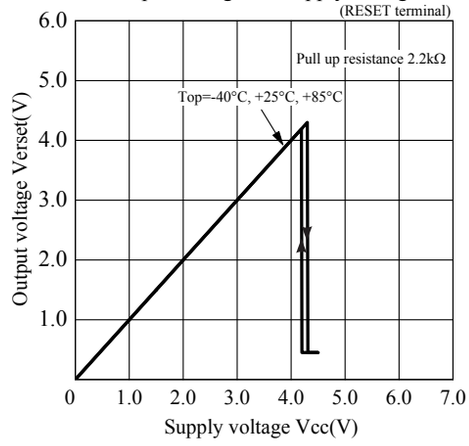


■Typical characteristic curves

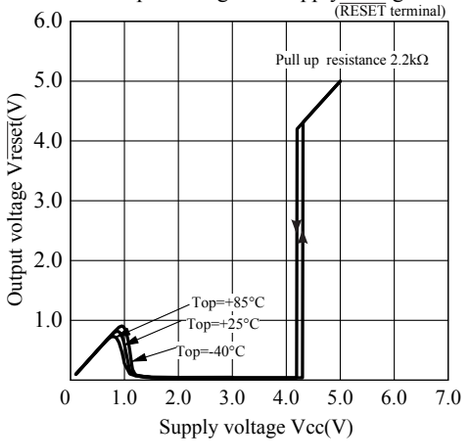
Supply current vs. Supply voltage



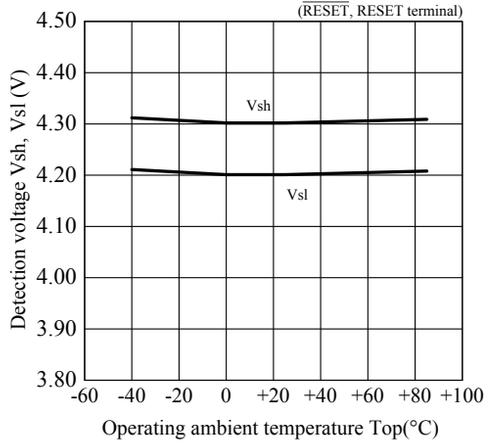
Output voltage vs. Supply voltage



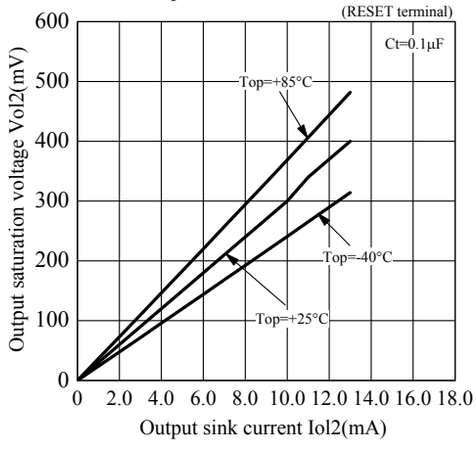
Output voltage vs. Supply voltage



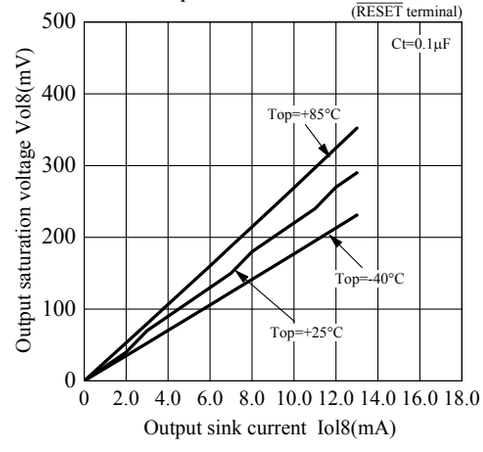
Detection voltage (Vsh, Vsl) vs.
Operating ambient temperature



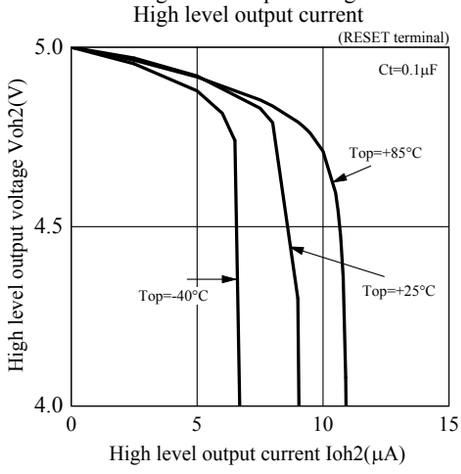
Output saturation voltage vs.
Output sink current



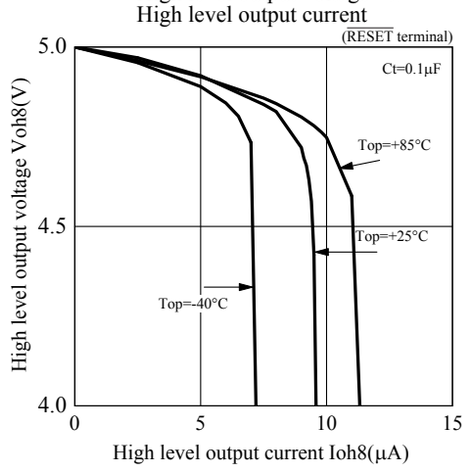
Output saturation voltage vs.
Output sink current



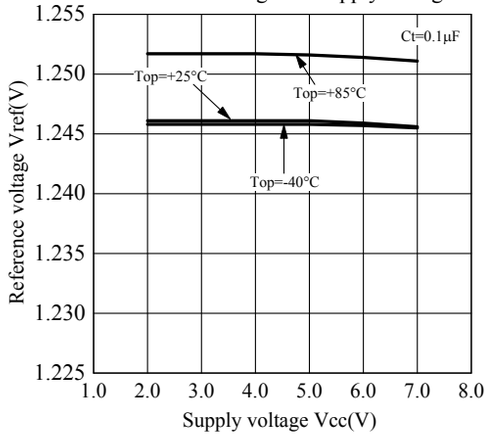
High level output voltage vs.
High level output current



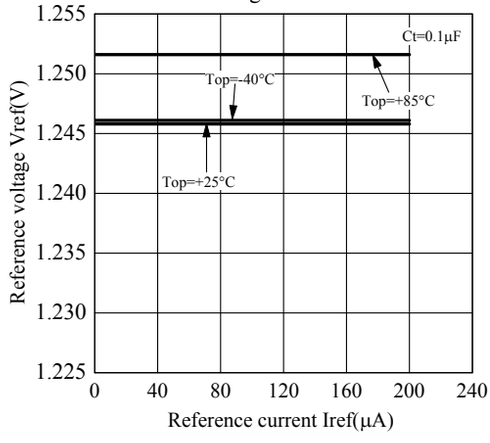
High level output voltage vs.
High level output current



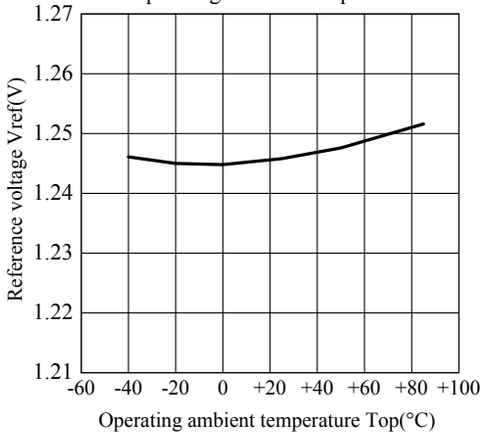
Reference voltage vs. Supply voltage



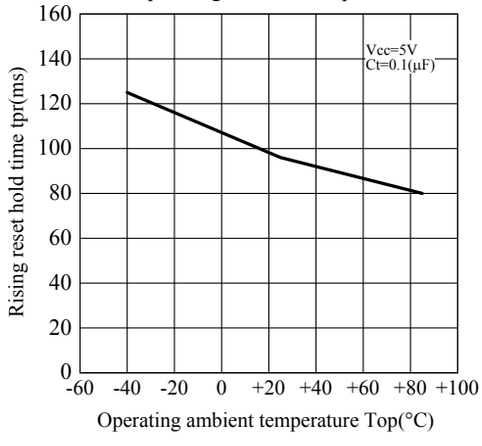
Reference voltage vs. Reference current



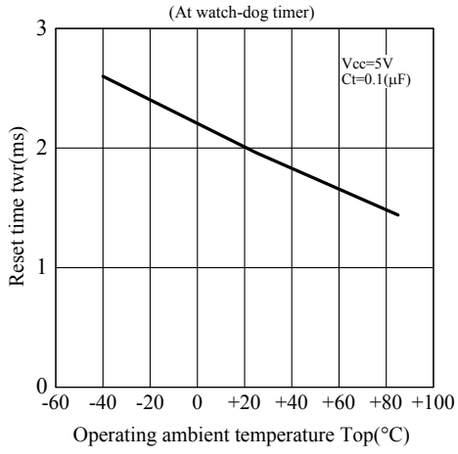
Reference voltage vs.
Operating ambient temperature



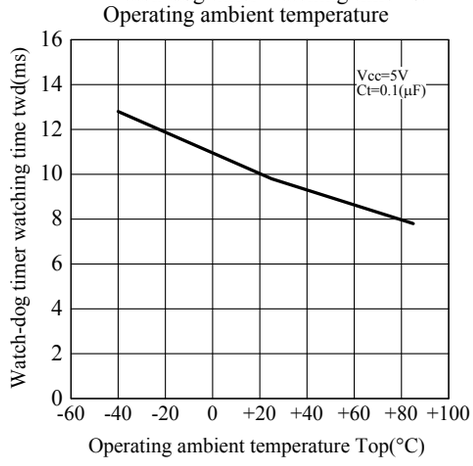
Rising reset hold time vs.
Operating ambient temperature



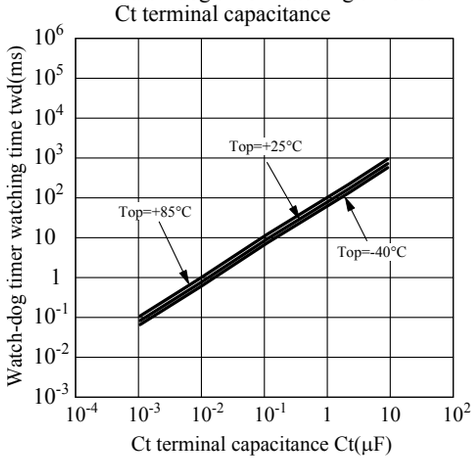
Reset time vs. Operating ambient temperature
(At watch-dog timer)



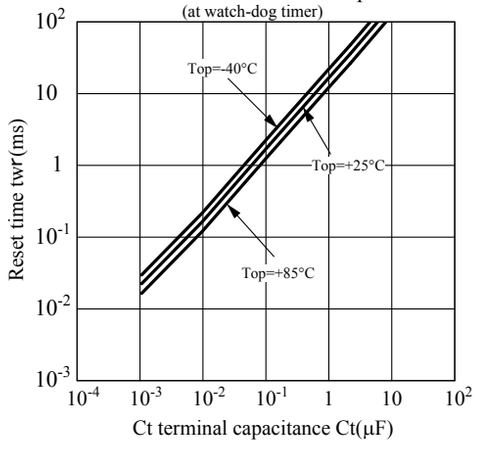
Watch-dog timer watching time vs.
Operating ambient temperature



Watch-dog timer watching time vs.
Ct terminal capacitance



Reset time vs. Ct terminal capacitance
(at watch-dog timer)



Rising reset hold time vs. Ct terminal capacitance