ELM7C3793xxxxA CMOS voltage detector with dual input watchdog timer

■General description

ELM7C3793 series is an integrated circuit to monitor power voltage; it incorporates a watchdog timer. A reset signal is output when the power is cut or falls abruptly. When the power recovers normally after resetting, a power-on reset signal is output to microprocessor units (MPUs). An internal watchdog timer with two inputs for system operation diagnosis can provide a fail-safe function for various application systems.The standard detection voltages are 3.0V, 3.7V, 4.2V and 4.5V; ELM7C3793 series can also be made as semi-custom IC within the range of 1.6V to 5.0V by 0.1V step.

■Features

- Detection voltage with hysteresis function.
- Integrated dual input watchdog timer.
- Watchdog-timer halt function (by inhibition pin).
- Independently-set watchdog and reset times
- Precise detection of power voltage fall : ±2.5%
- Low current consumption : Typ.31μA
- Package : SOP-8 150mil, SOP-8 208mil, SON8-3×3

■Application

- Reset for Microprocessor, etc.

■Maximum absolute ratings

Parameter		Symbol	Limit	Unit
Power supply		Vcc	6.5	V
Input Voltage	CK1	Vck1	Vss-0.3 to Vcc+0.3	V
	CK2	Vck2		
	INH	Vinh		
Reset output voltage	$\overline{\text{(RESET)}}$	Voh, Vol	Vss-0.3 to Vcc+0.3	V
Reset output current		Ioh, Iol	-10 to 10	mA
Power dissipation		Pd	300 (SOP-8)	mW
			500 (SON8-3×3)	
Operating temperature		Top	-40 to +85	°C
Storage temperature		Tstg	-55 to +125	°C

■Selection guide

ELM7C3793xxxxA-x

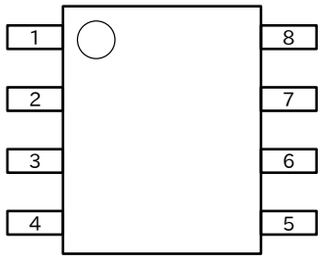
Symbol		
a, b	Detection voltage	e.g. : 30: Vsl=3.0V 37: Vsl=3.7V 42: Vsl=4.2V 45: Vsl=4.5V
c	Output form	A: CMOS output D: N-ch open-drain output
d	Package	D: SOP-8 150mil P: SOP-8 208mil G: SON8-3×3
e	Product version	A
f	Taping direction	S: SON8-3×3 (Refer to PKG file) N: SOP-8 (Refer to PKG file)

ELM7C3793 x x x x A - x
↑ ↑ ↑ ↑ ↑ ↑
a b c d e f

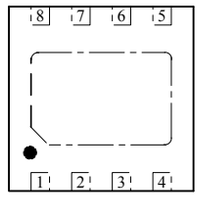
* Taping direction is one way.

■Pin configuration

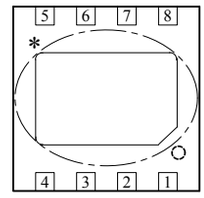
SOP-8(TOP VIEW)



SON8-3x3(TOP VIEW)



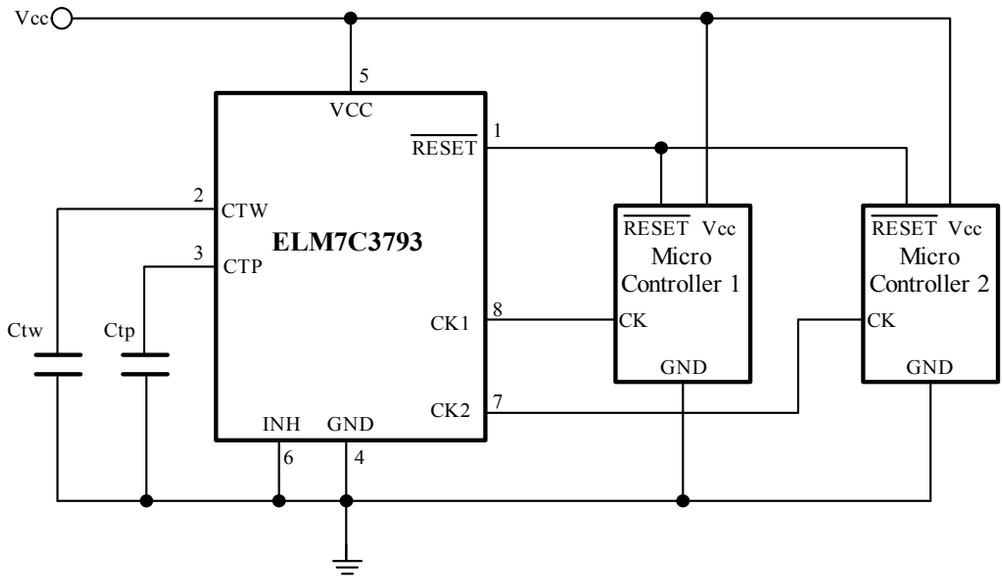
SON8-3x3(BOTTOM VIEW)



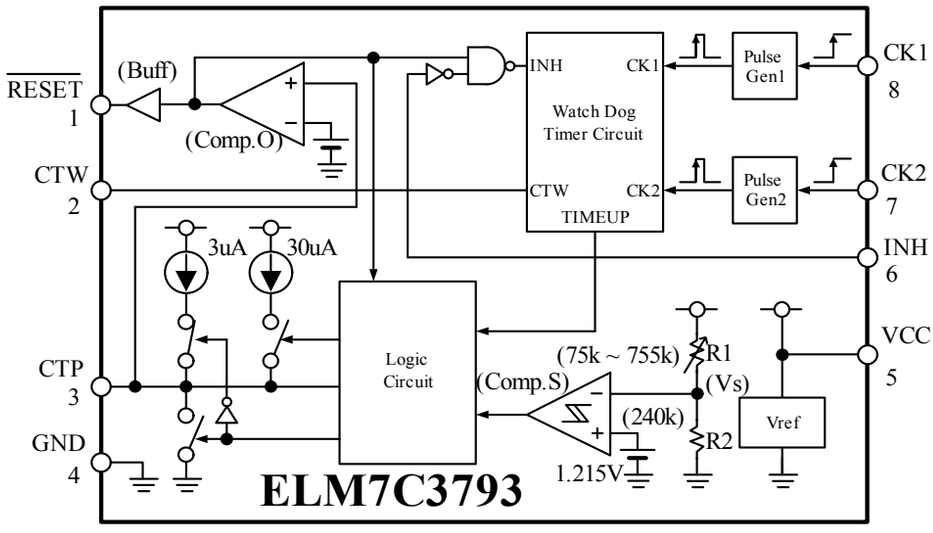
* The potential of the tab on the back is the ground(GND) level.
Please connect to GND pin(recommended) or set it to be open.

Pin No.	Pin name	Descriptions
1	$\overline{\text{RESET}}$	Outputs reset pin
2	CTW	Watchdog timer monitor time setting pin
3	CTP	Power-on reset hold time setting pin
4	GND	Ground pin
5	VCC	Power supply pin
6	INH	Inhibit pin
7	CK2	Inputs clock 2 pin
8	CK1	Inputs clock 1 pin

■Standard circuit



■Block diagram



■Functional descriptions

1. Comp.S

Comp.S is a comparator with hysteresis to compare the reference voltage with a voltage (Vs) that is the result of dividing the power voltage (Vcc) by resistors 1 and 2. When VS falls below 1.215V, a reset signal is output. This function enables the ELM7C379330xxA to detect an abnormality when the power is cut or falls abruptly.

2. Output circuit

The output circuit contains a $\overline{\text{RESET}}$ output control comparator that compares the voltage at the CTP pin to the threshold voltage to release the $\overline{\text{RESET}}$ output if the CTP pin voltage exceeds the threshold value.

Since the reset ($\overline{\text{RESET}}$) output buffer has CMOS organization, no pull-up resistor is needed.

3. Pulse generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 clock pins changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

4. Watchdog timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock pins to monitor a single clock pulse.

5. Inhibition pin

The inhibition (INH) pin forces the watchdog timer on/off. When this pin is High level, the watchdog timer is stopped.

6. Logic circuit

The logic circuit controls the charging and discharging of the power-on reset hold time setting capacitor(Ctp), and turns on/off the circuit that accelerates charging of the power-on reset hold time setting capacitor (Ctp) at a reset. The accelerate charging circuit operates only at a reset; it does not operate at a power-on reset when the power is turned on.

■Electrical characteristics

Vsl=3.7V(ELM7C379337xxA) Vcc=5.0V, Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	-	1.2	5.0	6.0	V
Power supply current	Icc	After exit from reset	-	30	50	μA
Detection voltage	Vsl	Vcc falling	3.60	3.70	3.80	V
		Top=-40℃ to +85℃	(3.55)*	3.70	(3.85)*	
	Vsh	Vcc rising	3.69	3.79	3.89	V
		Top=-40℃ to +85℃	(3.64)*	3.79	(3.94)*	
Detection voltage hysteresis difference	Vshys	Vsh-Vsl	40	85	130	mV
Clock-input threshold voltage	Vcih	CK rising	(1.0)*	1.6	2.5	V
	Vcil	CK falling	0.8	1.3	(2.0)*	
Clock-input hysteresis	Vchys	-	(0.1)*	0.3	(0.5)*	V
Inhibition-input voltage	Viih	-	3.5	-	Vcc	V
	Viil	-	0	-	0.8	
Input current (CK1, CK2, INH)	Iih	Vih=5.0V	-	0	1.0	μA
	Iil	Vil=0.0V	-1.0	0	-	
Reset output voltage	Voh*	I$\overline{\text{reset}}$=-5mA	4.50	4.75	-	V
	Vol	I$\overline{\text{reset}}$=+5mA	-	0.12	0.40	
Reset-output minimum power voltage	Vccl	I$\overline{\text{reset}}$=+50μA	-	0.8	1.2	V
Power-on reset hold time	tpr	Ctp=0.1μF*	30	75	120	ms
Watchdog timer monitor time	twd	Ctw=0.01μF *, Ctp=0.1μF	8	16	24	ms
Watchdog timer reset time	twr	Ctp=0.1μF	2.0	5.5	9.0	ms
Clock input pulse width	tckw	-	500	-	-	ns
Clock input pulse cycle	tckt	-	20	-	-	μs
Reset rising time	tr*	Cl=50pF	-	-	500	ns
Reset falling time	tf*		-	-	500	

* The values enclosed in parentheses ( ) are setting assurance values.

* Voh applies only to CMOS output.

* Ctp range is 0.001μF to 10μF, Ctw range is 0.001μF to 1μF.

* The voltage range is 10% to 90% at testing the reset output transition time.

Vsl=3.0V(ELM7C379330xxA) Vcc=3.3V, Top=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	-	1.2	3.3	6.0	V
Power supply current	Icc	After exit from reset	-	31	45	µA
Detection voltage	Vsl	Vcc falling	2.93	3.00	3.07	V
		Top=-40°C to +85°C	(2.89)*	3.00	(3.11)*	
	Vsh	Vcc rising	3.00	3.07	3.14	V
		Top=-40°C to +85°C	(2.96)*	3.07	(3.18)*	
Detection voltage hysteresis difference	Vshys	Vsh-Vsl	30	70	110	mV
Clock-input threshold voltage	Vcih	CK rising	(0.7)*	1.3	1.9	V
	Vcil	CK falling	0.5	1.0	(1.5)*	
Clock-input hysteresis	Vchys	-	(0.1)*	0.3	(0.6)*	V
Inhibition-input voltage	Viih	-	2.2	-	Vcc	V
	Viil	-	0	-	0.8	
Input current (CK1, CK2, INH)	Iih	Vih=3.3V	-	0	1.0	µA
	Iil	Vil=0.0V	-1.0	0	-	
Reset output voltage	Voh*	$I\overline{reset}$=-3mA	2.80	3.10	-	V
	Vol	$I\overline{reset}$=+3mA	-	0.12	0.40	
Reset-output minimum power voltage	Vccl	$I\overline{reset}$=+50µA	-	0.8	1.2	V
Power-on reset hold time	tpr	Ctp=0.1µF*	30	75	120	ms
Watchdog timer monitor time	twd	Ctw=0.01µF *, Ctp=0.1µF	8	16	24	ms
Watchdog timer reset time	twr	Ctp=0.1µF	2.0	5.5	9.0	ms
Clock input pulse width	tckw	-	500	-	-	ns
Clock input pulse cycle	tckt	-	20	-	-	µs
Reset rising time	tr*	Cl=50pF	-	-	500	ns
Reset falling time	tf*		-	-	500	

* The values enclosed in parentheses ( ) are setting assurance values.
* Voh applies only to CMOS output.
* Ctp range is 0.001µF to 10µF, Ctw range is 0.001µF to 1µF.
* The voltage range is 10% to 90% at testing the reset output transition time.

■Timing chart

Fig.1: Basic operation (Positive clock pulse)

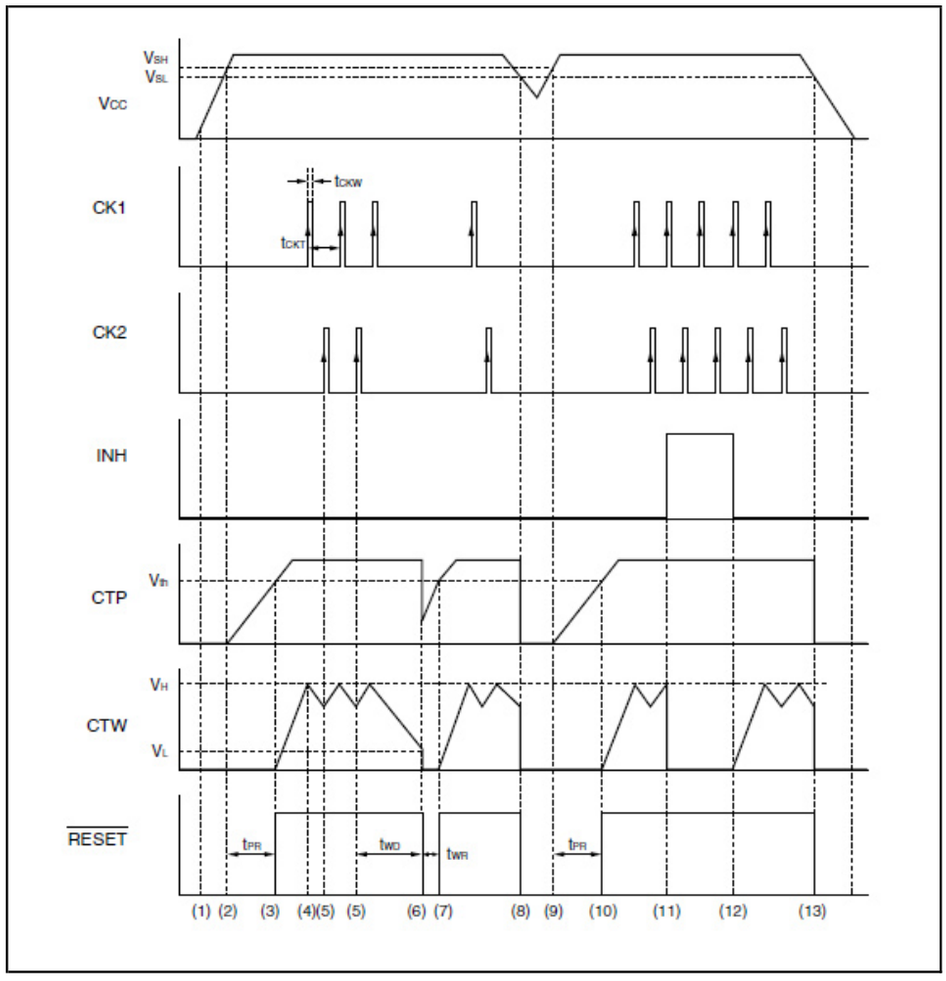


Fig.2: Basic operation (Negative clock pulse)

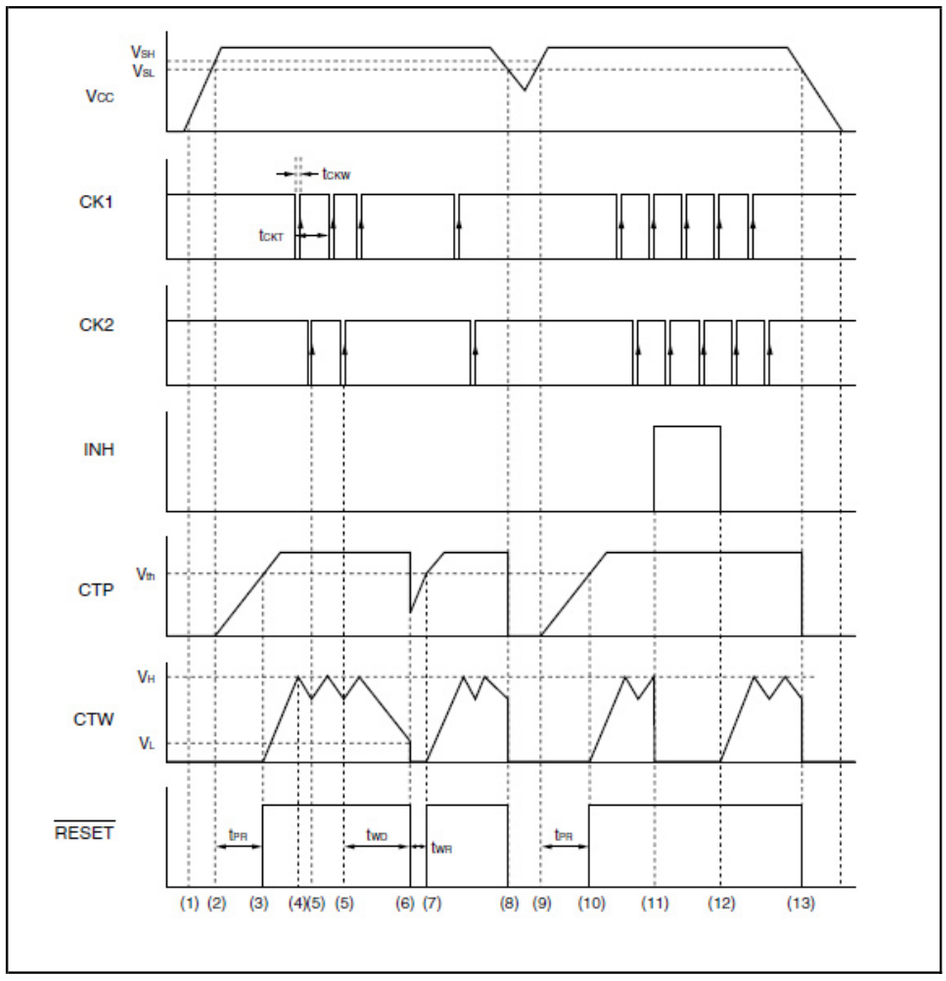


Fig.3: Single-clock input monitoring (Positive clock pulse)

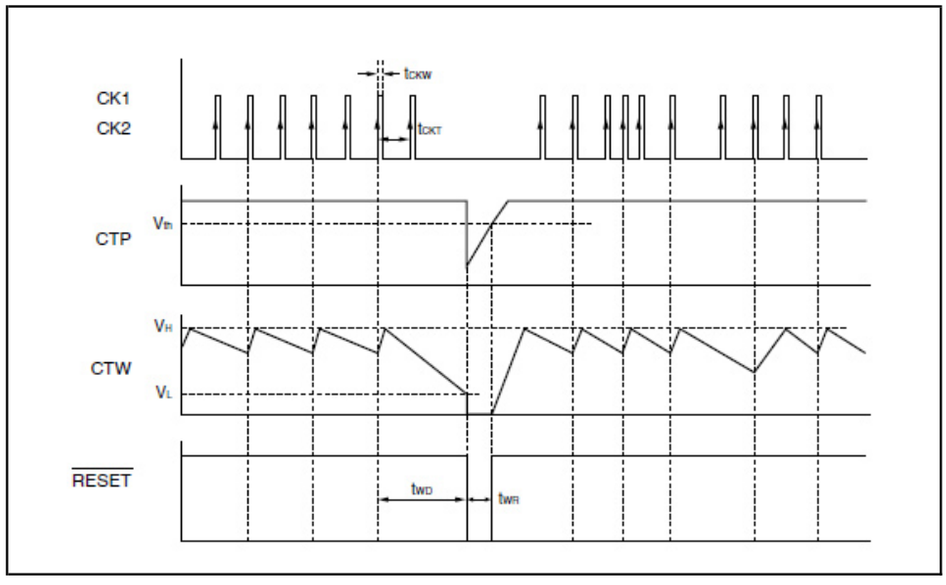


Fig.4: Inhibition operation (Positive clock pulse)

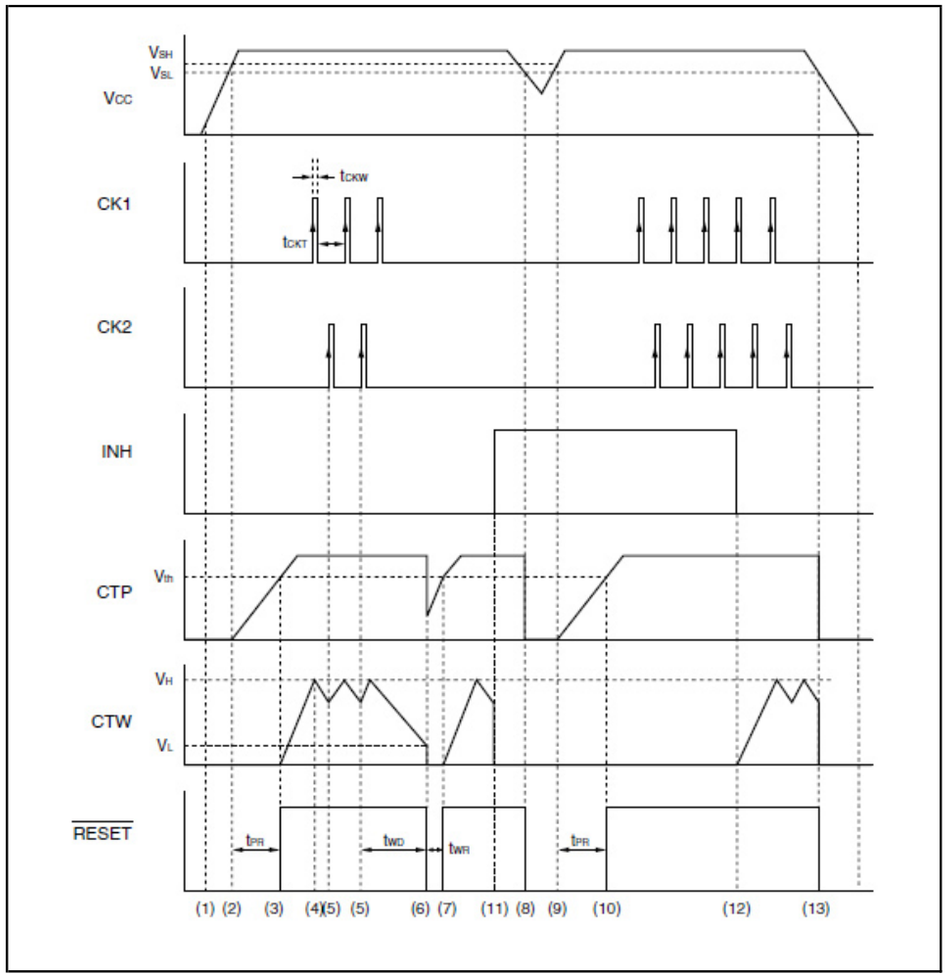
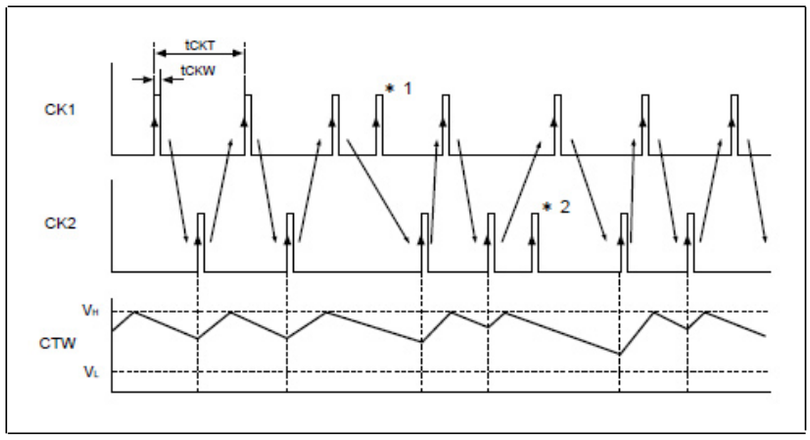


Fig.5: Clock pulse input supplementation (Positive clock pulse)



Note :

The ELM7C3793 watchdog timer monitors Clock1 (CK1) and Clock2 (CK2) pulses alternately.

When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (Ctw) switches to charging from discharging.

When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored.

In the above figure, pulse *1 and *2 are ignored.

■Operation sequence

1.Positive clock pulse input

See “Fig.1 Basic operation (positive clock pulse)” under “■Timing chart”.

2. Negative clock pulse input

See “Fig.2 Basic operation (negative clock pulse)” under “■Timing chart”.

ELM7C3793 operates in the same way whether it inputs positive or negative pulses.

3. One clock monitoring

To use ELM7C3793 while monitoring only one clock, connect clock pins CK1 and CK2.

Although ELM7C3793 operates basically in the same way as when monitoring two clocks, it monitors the clock signal at every other input pulse.

See “Fig.3 Single-clock input monitoring (positive clock pulse)” under “■Timing chart”.

4. Description of operations

The numbers given to the following items correspond to numbers (1) to (13) used in “■Timing chart”.

(1) ELM7C3793 outputs a reset signal when the supply voltage (Vcc) reaches about 0.8 V (Vccl).

(2) If Vcc reaches or exceeds the rise-time detected voltage Vsh, ELM7C3793 starts charging the power-on reset hold time setting capacitor Ctp. At this time, the output remains in a reset state. The Vsh value is about 3.07V(Typ.).

(3) When Ctp has been charged for a certain period of time Tpr (until the CTP pin voltage exceeds the threshold voltage (Vth) after the start of charging), ELM7C3793 cancels the reset (setting the $\overline{\text{RESET}}$ pin to “H” level from “L” level). The Vth value is about 1.245V(Typ.) regardless of Vcc voltage.

The power-on reset hold time tpr is set with the following equation:

$$tpr(ms) \approx A \times Ctp(\mu F)$$

The value of A is about 750 regardless of Vcc voltage. ELM7C3793 also starts charging the watchdog time setting capacitor (Ctw).

(4) When the voltage at the watchdog timer monitor time setting pin CTW reaches the “H” level threshold voltage Vh, the Ctw switches from the charge state to the discharge state. The value of Vh is always about 1.245 V regardless of Vcc voltage.

(5) If the CK2 pin inputs a clock pulse (positive edge trigger) when the Ctw is being discharged in the CK1-CK2 order or simultaneously, the Ctw switches from the discharge state to the charge state. ELM7C3793 repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses with the system logic circuit operating normally.

(6) If no clock pulse is fed to the CK1 or CK2 pin within the watchdog timer monitor time twd due to some problem with the system logic circuit, the CTW pin is set to the “L” level threshold voltage Vl or less and ELM7C3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to “L” level from “H” level).

The watchdog timer monitor time twd is set with the following equation:

$$twd(ms) \approx B \times Ctw(\mu F)$$

The value of B is hardly affected by the power supply voltage; it is about 1600 regardless of Vcc voltage.

(7) When a certain period of time twr has passed (until the CTP pin voltage reaches or exceeds Vth again after recharging the Ctp), ELM7C3793 cancels the reset signal and starts operating the watchdog timer. The watchdog timer monitor reset time twr is set with the following equation:

$$twr\ (ms) \approx D \times Ctp(\mu F)$$

The value of D is 55 regardless of Vcc voltage.

ELM7C3793 repeats operations. (4) and (5) as long as the CK1/CK2 pin inputs clock pulses. If no clock pulse is input, ELM7C3793 repeats operations (6) and (7).

(8) If Vcc is lowered to the fall-time detected voltage (Vsl) or less, the CTP pin voltage decreases and ELM7C3793 outputs a reset signal (setting the $\overline{\text{RESET}}$ pin to "L" level from "H" level). The value of Vsl is 3.0 V
(9) When Vcc reaches or exceeds Vsh again, ELM7C3793 starts charging the Ctp.
(10) When the CTP pin voltage reaches or exceeds Vth, ELM7C3793 cancels the reset and restarts operating the watchdog timer. It repeats operations (4) and (5) as long as the CK1/CK2 pin inputs clock pulses.
(11) Making the inhibit pin active (setting the INH pin to "H" from "L") forces the watchdog timer to stop operation. This stops only the watchdog timer, leaving ELM7C3793 monitoring Vcc (operations (8) to (10)). The watchdog timer remains inactive unless the inhibit input is canceled.
(12) Canceling the inhibit input (setting the INH pin to "L" from "H") restarts the watchdog timer.
(13) The reset signal is output when the power supply is turned off to set Vcc to Vsl or less.
(14) Equation of time-setting capacitances (Ctp and Ctw) and setting time:

$tpr\ [ms] \approx A \times Ctp\ [\mu F]$
$twd\ [ms] \approx B \times Ctw\ [\mu F]$
$twr\ [ms] \approx D \times Ctp\ [\mu F]$

Values of A, B and D

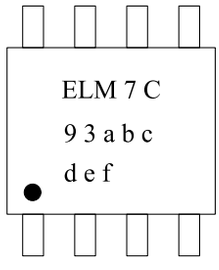
Product name	A	B	D
ELM7C3793xxxxA	750	1600	55

Setting example (When Ctp=0.1μF, Ctw=0.01μF)

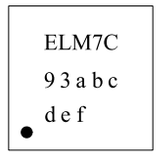
Product name	tpr[ms]	twd[ms]	twr[ms]
ELM7C3793xxxxA	75	16	5.5

■Marking

SOP-8



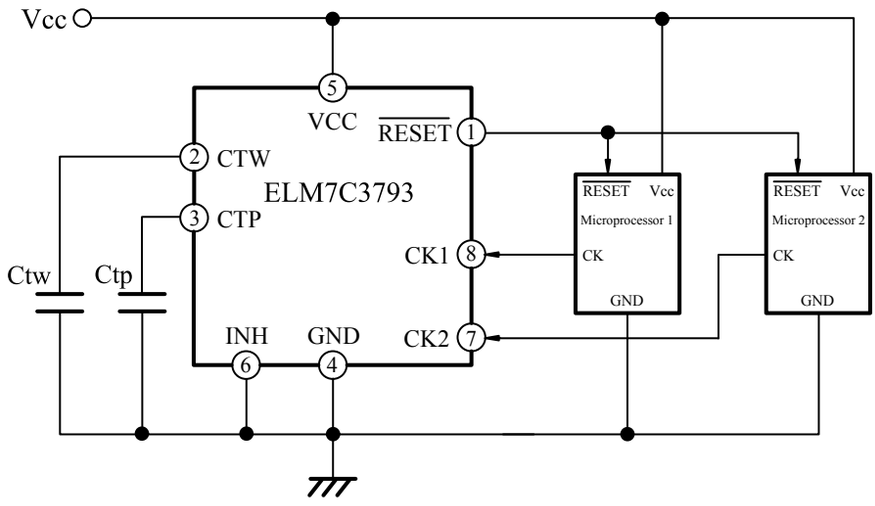
SON8-3×3



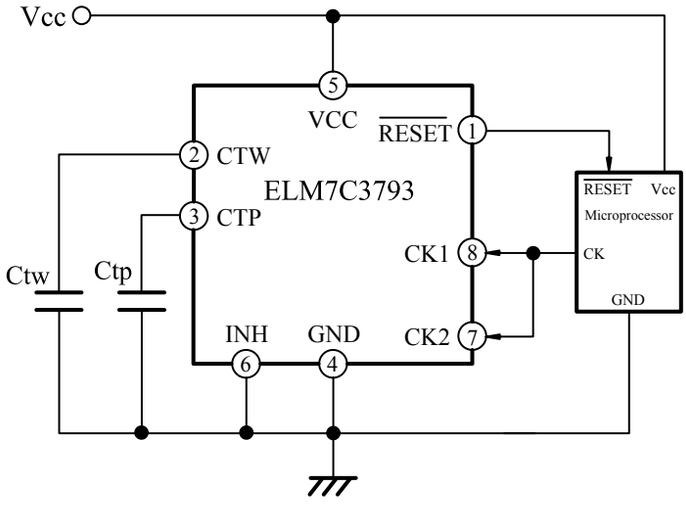
Symbol	Mark	Content
a, b	0 to 9	Detection voltage
c	A or D	Output form
d	0 to 9	Last numeral of A.D.
e	A to M (excepted I.)	Assembly month
f	0 to 9	Lot No.

■Application circuit example

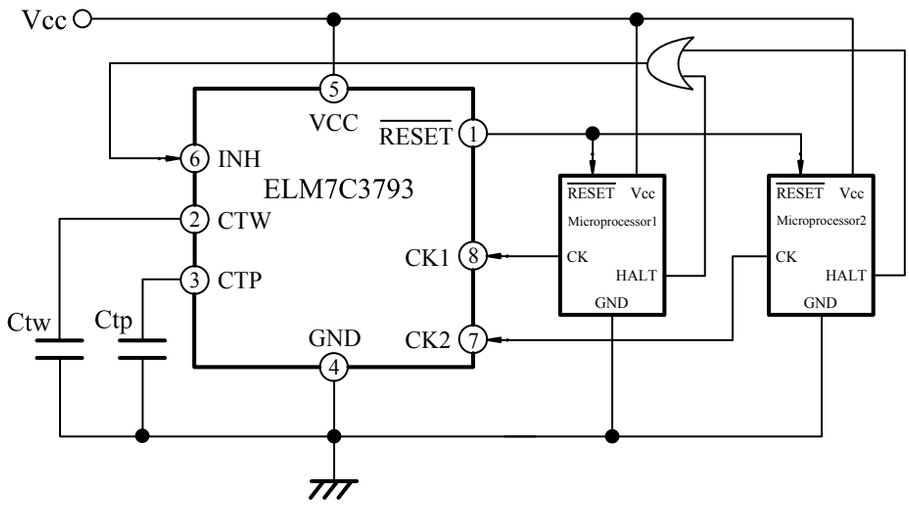
1) Supply voltage monitor and watchdog timer (2 clocks monitoring)



2) Supply voltage monitor and watchdog timer (1 clock monitoring)

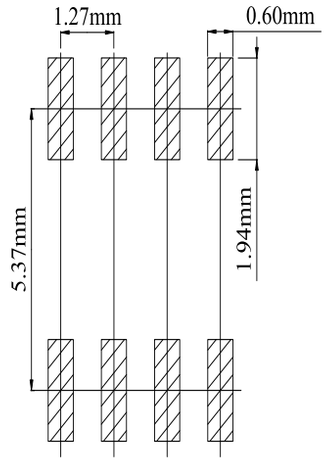


3) Supply voltage monitor and watchdog timer stop

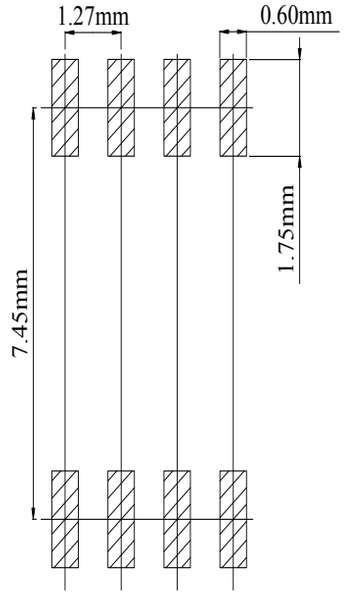


■Reference land pattern

SOP-8 150mil

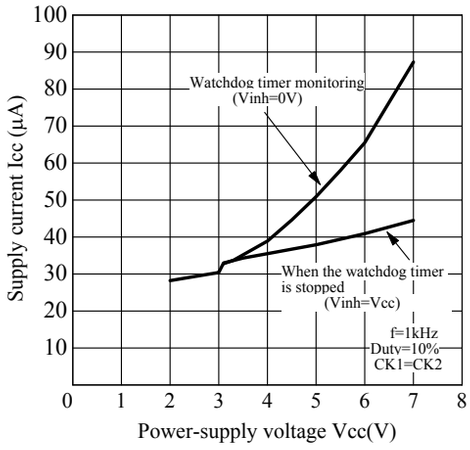


SOP-8 208mil

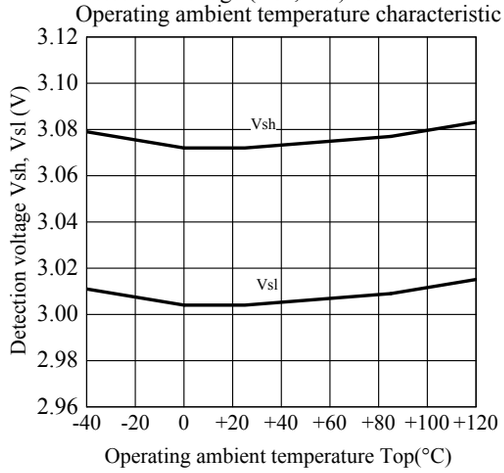


■Typical Characteristics

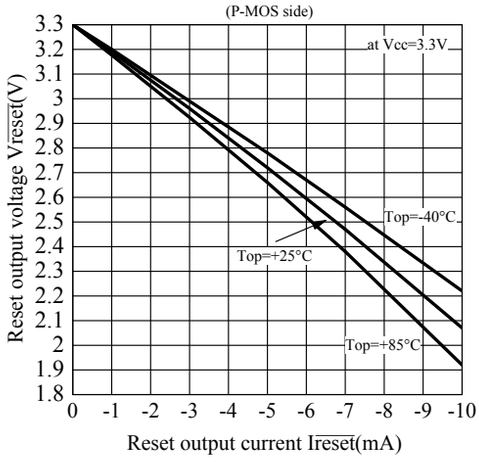
Power supply current vs. Power supply voltage



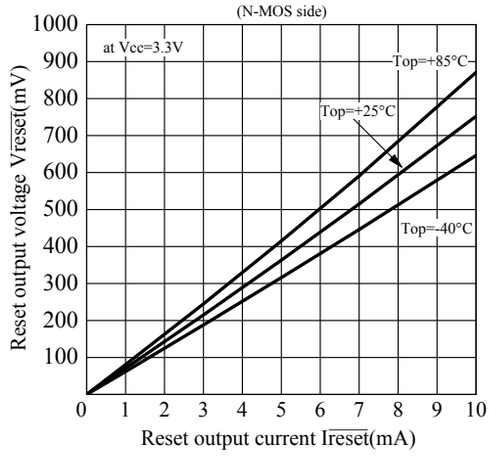
Detection voltage (Vsh, Vsl) vs.
Operating ambient temperature characteristic



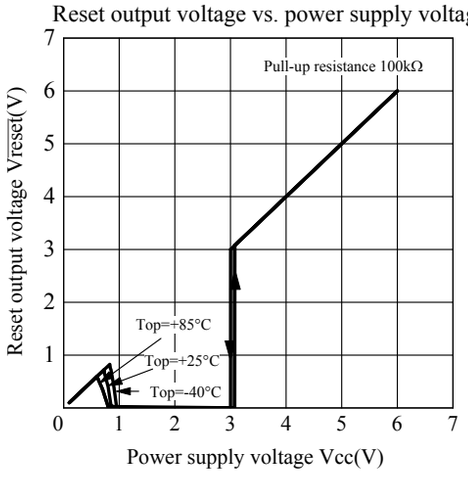
Reset output voltage vs. reset output current
(P-MOS side)



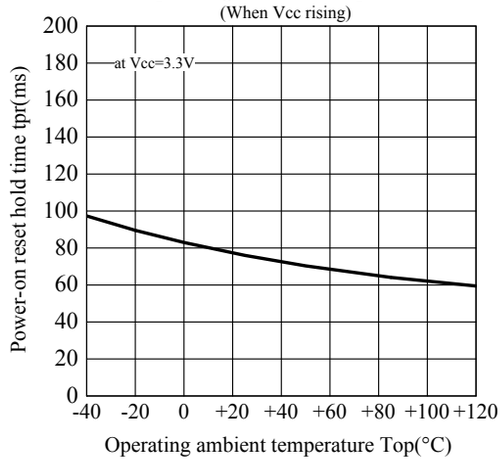
Reset output voltage vs. reset output current
(N-MOS side)



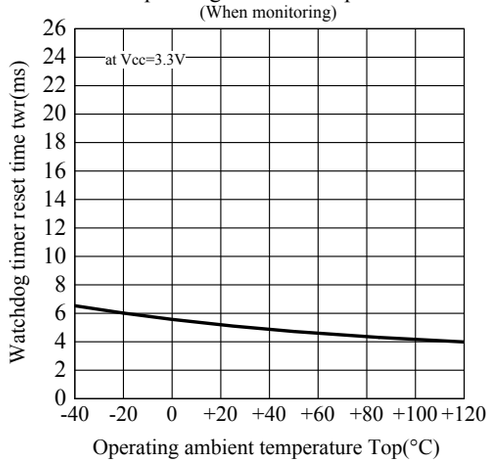
Reset output voltage vs. power supply voltage



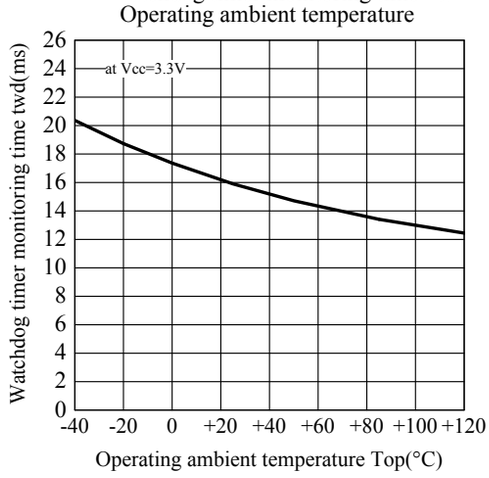
Power-on reset hold time vs.
Operating ambient temperature
(When Vcc rising)



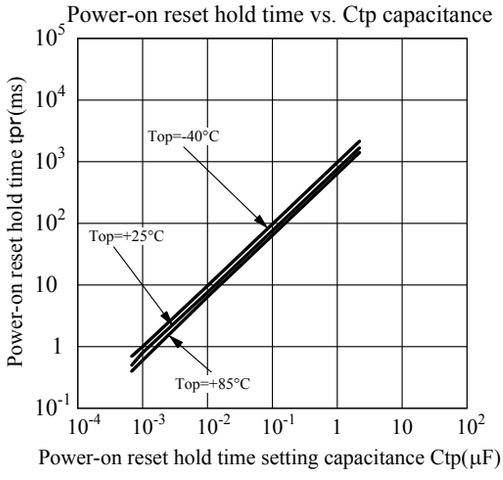
Watchdog timer reset time vs.
Operating ambient temperature
(When monitoring)



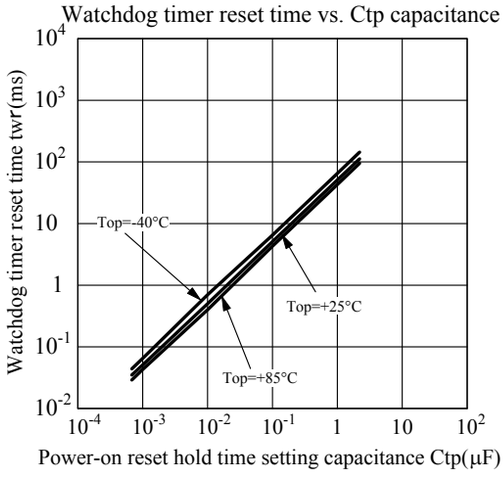
Watchdog timer monitoring time vs.
Operating ambient temperature



Power-on reset hold time vs. Ctp capacitance



Watchdog timer reset time vs. Ctp capacitance



Watchdog timer monitoring time vs. Ctw capacitance