

单 N 沟道 MOSFET

ELM52306AEA-S

<http://www.elm-tech.com>

■概要

ELM52306AEA-S 是 N 沟道低输入电容，低工作电压，低导通电阻的大电流 MOSFET。另外，此芯片还内藏 ESD 保护电路。

■特点

- $V_{ds}=20V$
- $I_d=1.8A$ ($V_{gs}=4.5V$)
- $R_{ds(on)} = 280m\Omega$ ($V_{gs}=4.5V$)
- $R_{ds(on)} = 340m\Omega$ ($V_{gs}=2.5V$)
- $R_{ds(on)} = 750m\Omega$ ($V_{gs}=1.8V$)
- ESD 保护

■绝对最大额定值

如没有特别注明时, $T_a=25^\circ C$

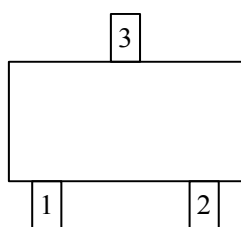
项目	记号	规格范围	单位
漏极 - 源极电压	V_{ds}	20	V
栅极 - 源极电压	V_{gs}	± 12	V
漏极电流 ($T_j=150^\circ C$)	Id	$T_a=25^\circ C$	1.8
		$T_a=70^\circ C$	1.2
漏极电流 (脉冲)	I_{dm}	6	A
容许功耗	Pd	$T_c=25^\circ C$	1.25
		$T_c=70^\circ C$	0.80
动作结合部温度	T_j	150	$^\circ C$
保存温度范围	T_{stg}	- 55 ~ 150	$^\circ C$

■热特性

项目	记号	典型值	最大值	单位
最大结合部 - 环境热阻	$R_{\theta ja}$		120	$^\circ C/W$

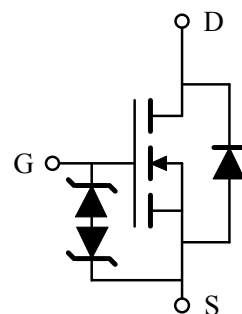
■引脚配置图

SOT-23(俯视图)



引脚编号	引脚名称
1	GATE
2	SOURCE
3	DRAIN

■电路图



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■电特性

如没有特别注明时, Ta=25℃

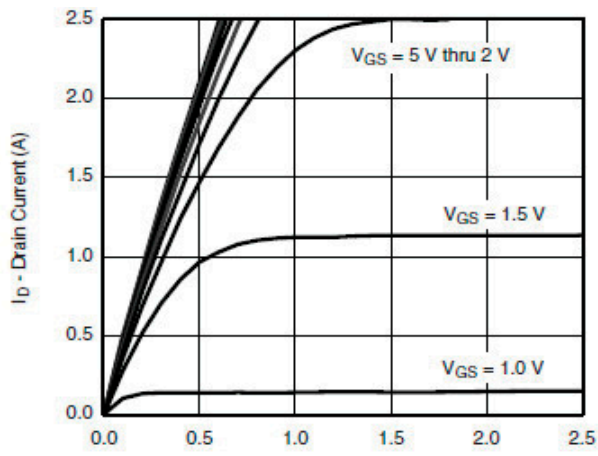
项目	记号	条件	最小值	典型值	最大值	单位
静态特性						
漏极 - 源极击穿电压	BV _{dss}	I _d =250μA, V _{gs} =0V	20			V
栅极接地时漏极电流	I _{dss}	V _{ds} =16V, V _{gs} =0V			1	μA
		V _{ds} =16V, V _{gs} =0V, Ta=85℃			5	
栅极漏电流	I _{gss}	V _{ds} =0V, V _{gs} =±12V			±1	mA
栅极阈值电压	V _{gs(th)}	V _{ds} =V _{gs} , I _d =250μA	0.3		0.8	V
导通时漏极电流	I _{d(on)}	V _{gs} =4.5V, V _{ds} ≥5V	1.8			A
漏极 - 源极导通电阻	R _{ds(on)}	V _{gs} =4.5V, I _d =1.8A		220	280	mΩ
		V _{gs} =2.5V, I _d =1.5A		260	340	
		V _{gs} =1.8V, I _d =1.2A		540	750	
正向跨导	G _{fs}	V _{ds} =10V, I _d =1.0A		1		S
二极管正向压降	V _{sd}	I _s =1.0A, V _{gs} =0V		0.65	1.20	V
寄生二极管最大连续电流	I _s				1	A
动态特性						
输入电容	C _{iss}	V _{gs} =0V, V _{ds} =10V, f=1MHz		70		pF
输出电容	C _{oss}			20		pF
反馈电容	C _{rss}			8		pF
开关特性						
总栅极电荷	Q _g	V _{gs} =4.5V, V _{ds} =10V, I _d ≐1.2A		1.06	1.38	nC
栅极 - 源极电荷	Q _{gs}			0.18		nC
栅极 - 漏极电荷	Q _{gd}			0.32		nC
导通延迟时间	t _{d(on)}	V _{gs} =4.5V, V _{ds} =10V R _L =20Ω, I _d ≐1.2A R _{gen} =1Ω		18	26	ns
导通上升时间	t _r			20	28	ns
关闭延迟时间	t _{d(off)}			70	110	ns
关闭下降时间	t _f			25	40	ns

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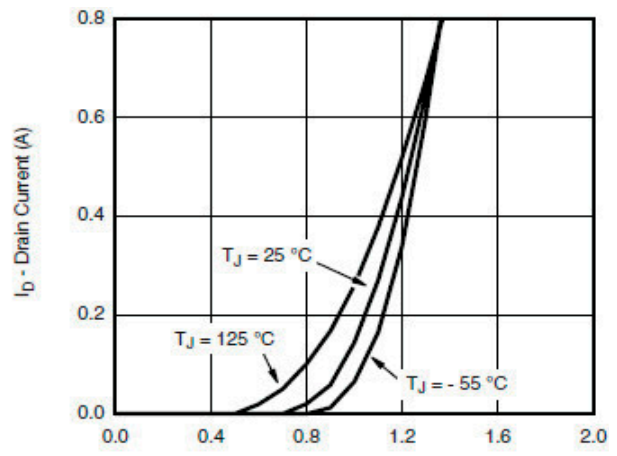
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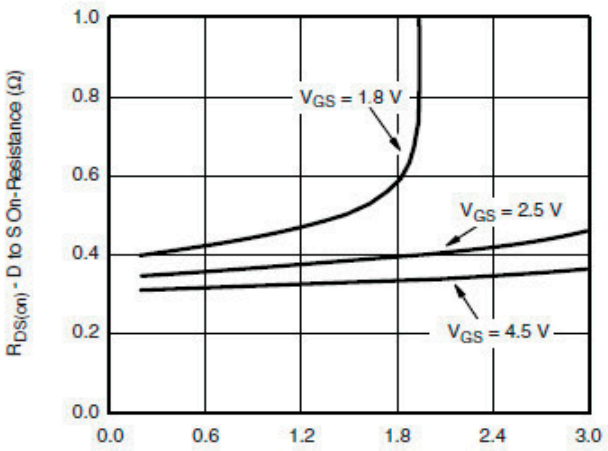
■ 标准特性和热特性曲线



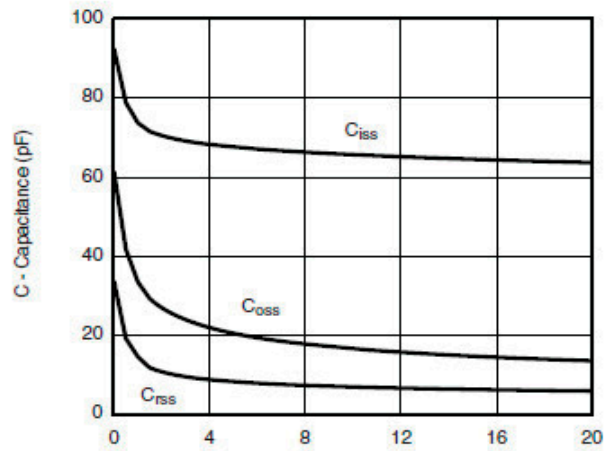
Output Characteristics



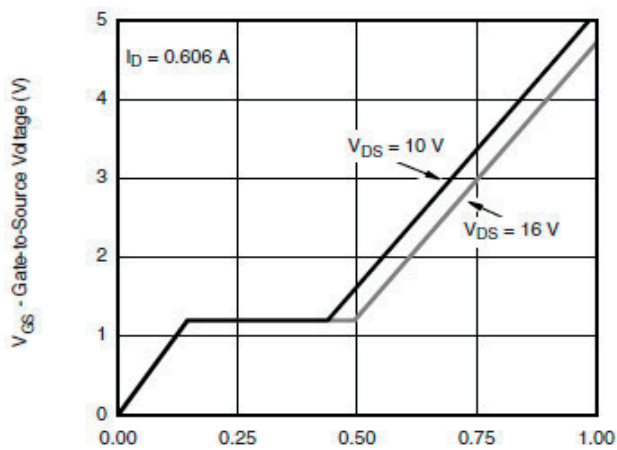
Transfer Characteristics



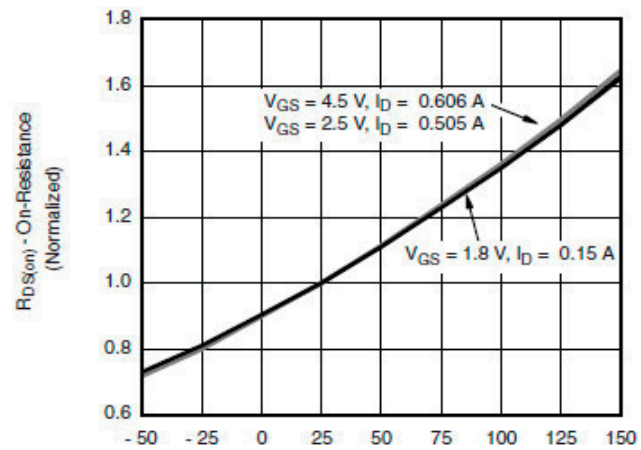
On-Resistance vs. Drain Current



Capacitance



Gate Charge

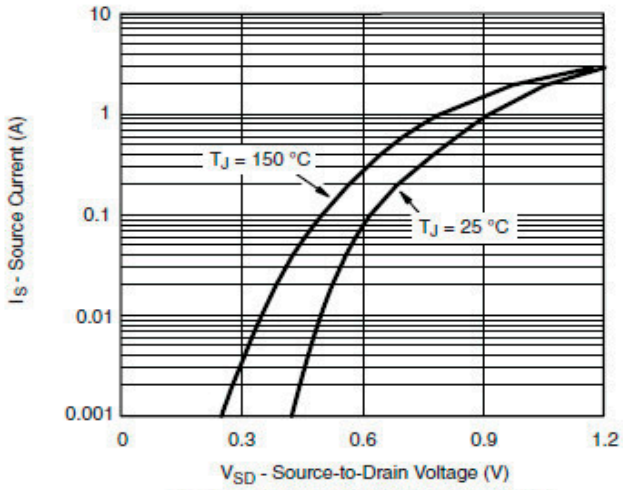


On-Resistance vs. Junction Temperature

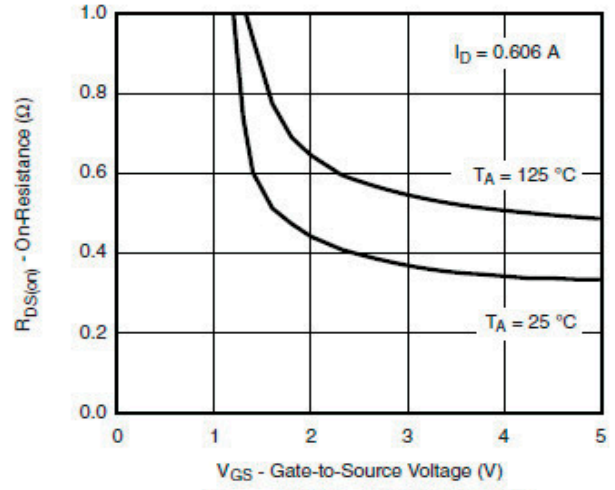
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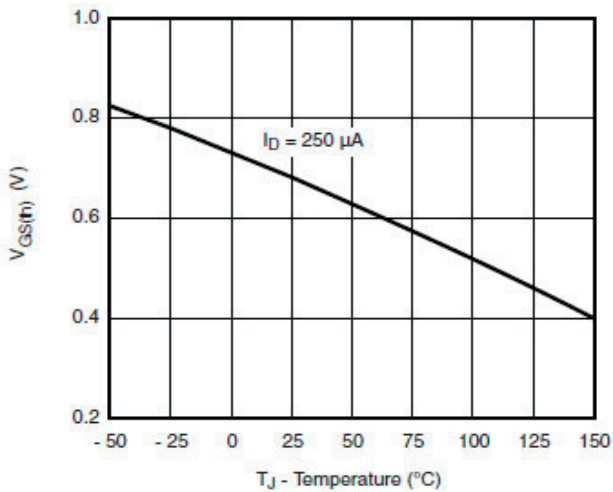
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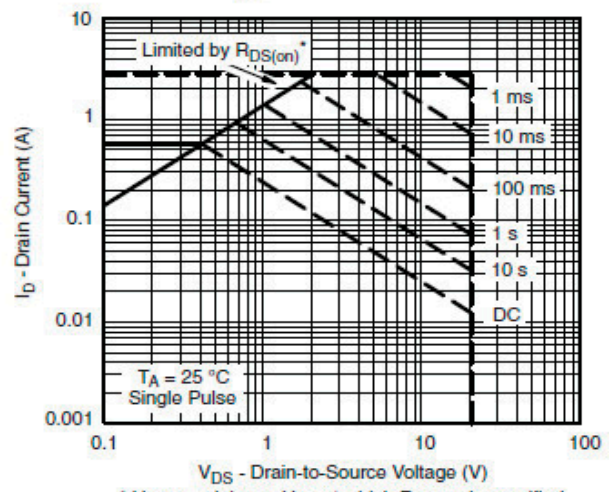
Source-Drain Diode Forward Voltage



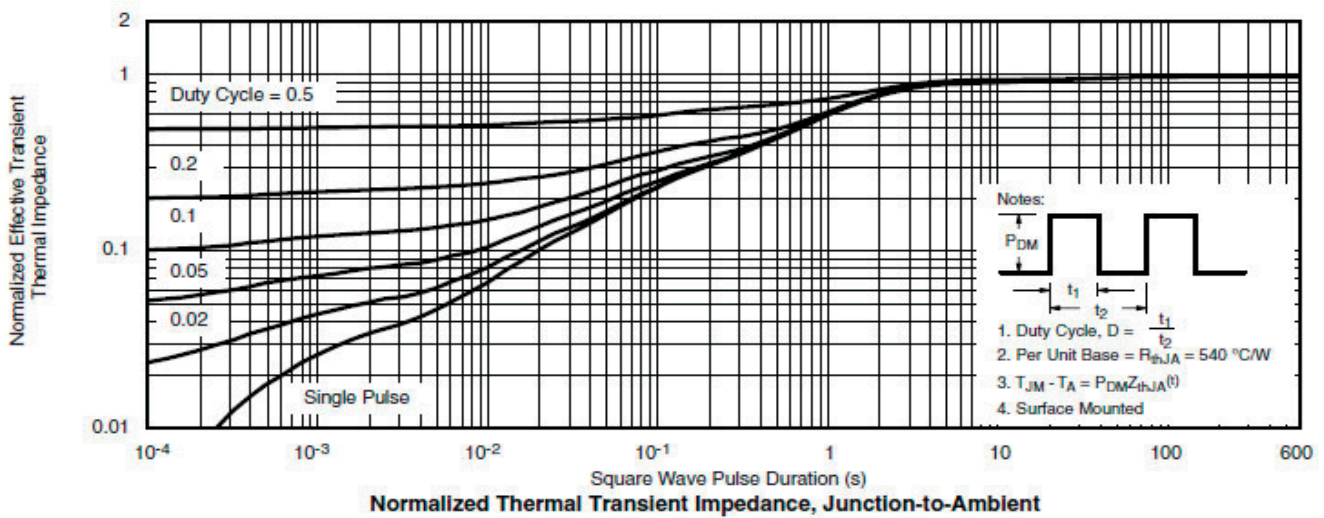
$R_{DS(on)}$ vs. V_{GS} vs Temperature



Threshold Voltage



Safe Operating Area, Junction-to-Ambient



- Notes:
- 1. Duty Cycle, $D = \frac{t_1}{t_2}$
 - 2. Per Unit Base = $R_{\theta JA} = 540 \text{ } ^\circ\text{C/W}$
 - 3. $T_{JM} - T_A = P_{DM} Z_{\theta JA}(t)$
 - 4. Surface Mounted

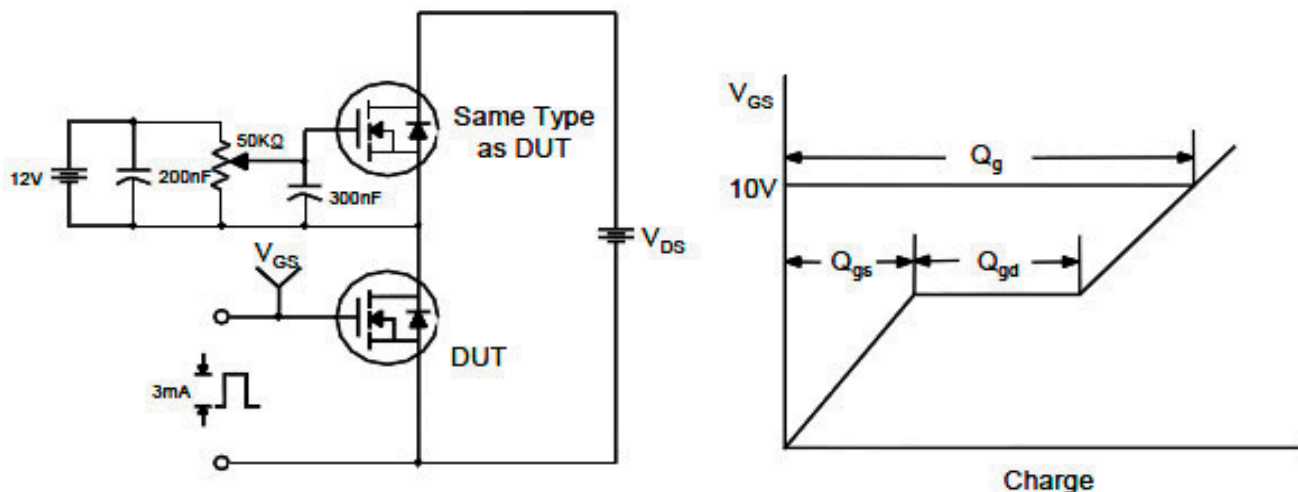
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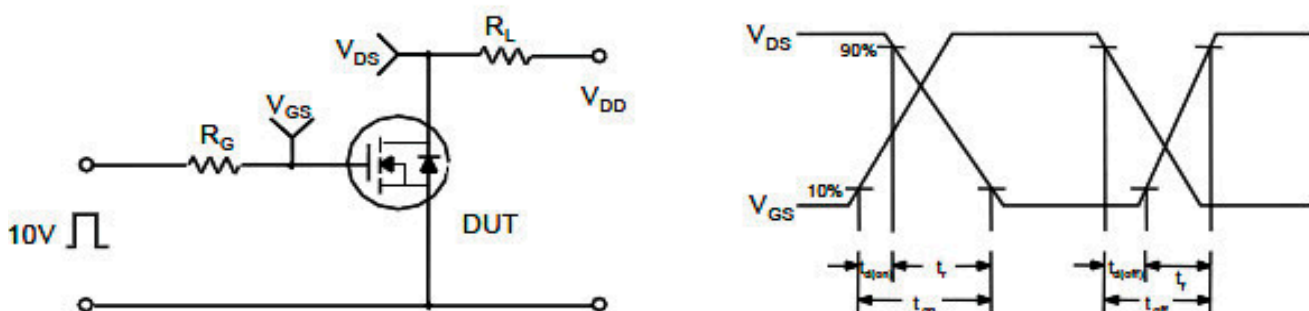
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■ 测试电路和波形

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

