# GD25B257D

# DATASHEET

# Contents

# 1. FEATURES

- 256M-bit Serial Flash
  - 32M-Byte
  - 256-Byte per programmable page
- Standard, Dual, Quad SPI, DTR
  - Standard SPI: SCLK, CS#, SI, SO, RESET#
  - Dual SPI: SCLK, CS#, IO0, IO1, RESET#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - SPI DTR (Double Transfer Rate) Read
  - On-chip ECC (1-bit correction every 8-Byte) (1)
  - 3 or 4-Byte Addressing Mode
- High Speed Clock Frequency

  -Maximum 104MHz for fast read on 3.0 - 3.6V power supply
  - Dual I/O Data transfer up to 208Mbits/s
  - Quad I/O Data transfer up to 416Mbits/s
  - DTR Quad I/O Data transfer up to 640Mbits/s

  -Maximum 80MHz for fast read on 2.7 - 3.0V power supply
  - Dual I/O Data transfer up to 160Mbits/s
  - Quad I/O Data transfer up to 320Mbits/s
  - DTR Quad I/O Data transfer up to 560Mbits/s
- Software Write Protection

  -Write protect all/portion of memory via software

  -Top/Bottom Block protection
- Allows XIP (eXecute In Place) Operation
  - Continuous Read With 8/16/32/64-Byte Wrap
- Fast Program/Erase Speed
  - Page Program time: 0.6ms typical
  - Sector Erase time: 70ms typical
  - Block Erase time: 0.2/0.3s typical
  - Chip Erase time: 100s typical
- Flexible Architecture
  - Uniform Sector of 4K-Byte
  - Uniform Block of 32/64K-Byte
- Low Power Consumption

  -1uA typical deep power down current

  -12uA typical standby current
- Advanced Security Features
  - 3x2048-Byte Security Registers With OTP Locks
  - 128-bit Unique ID
  - Serial Flash Discoverable parameters (SFDP) register
- Single Power Supply Voltage
  - Full voltage range: 2.7 - 3.6V
- Endurance and Data Retention
  - 20-year data retention typical
  - Minimum 100,000 Program/Erase Cycles
- Package Information
  - SOP16 (300mil)
  - WSON8 (8x6mm)
  - TFBGA-24 (5x5 ball array)

Note:

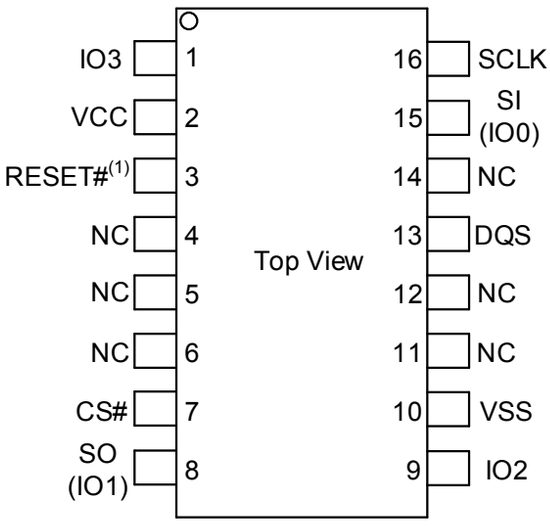
1. When ECC is enabled, it is required to program minimum one or multiple aligned 8-Byte granularities. Every aligned 8-Byte granularity should only be programmed once before Erase to ensure correct ECC operations.

# 2. GENERAL DESCRIPTION

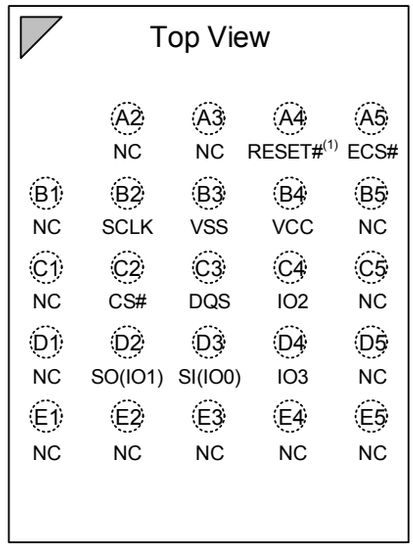
The GD25B257D (256M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, and I/O3 . The Dual I/O data is transferred with speed of 208Mbits/s and the Quad I/O & Quad output data is transferred with speed of 416Mbits/s, and the DTR Quad I/O data is transferred with speed of 640Mbits/s.

## CONNECTION DIAGRAM

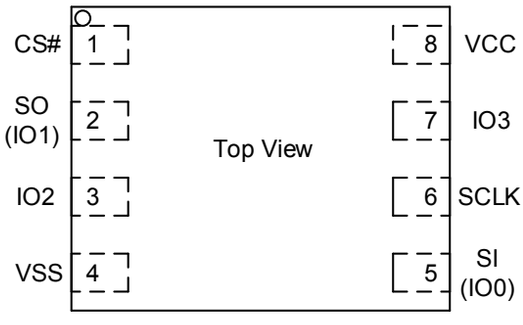
**Figure 1. Connection Diagram**




16-LEAD SOP




24-BALL TFBGA (5x5 ball array)




8 – LEAD WSON

Note:

1. Only for special order, Pin 3 of 16-LEAD SOP package or Pin A4 of 24-BALL TFBGA (5x5 ball array) package is RESET# pin. Please contact GigaDevice for detail
2. CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

## PIN DESCRIPTION

**Table 1. Pin Description for SOP16 package**

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | IO3 | I/O | Data Input Output 3 |
| 2 | VCC | | Power Supply |
| 3 | RESET# (1) | I | Reset Input |
| 7 | CS# | I | Chip Select Input |
| 8 | SO (IO1) | I/O | Data Output (Data Input Output 1) |
| 9 | IO2 | I/O | Data Input Output 2 |
| 10 | VSS | | Ground |
| 13 | DQS | O | Data Strobe Signal Output |
| 15 | SI (IO0) | I/O | Data Input (Data Input Output 0) |
| 16 | SCLK | I | Serial Clock Input |

**Table 2 Pin Description for TFBGA24 5*5package**

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| A4 | RESET# (1) | I | Reset Input |
| A5 | ECS# | O | ECC Correction Signal |
| B2 | SCLK | I | Serial Clock Input |
| B3 | VSS | | Ground |
| B4 | VCC | | Power Supply |
| C2 | CS# | I | Chip Select Input |
| C3 | DQS | O | Data Strobe Signal Output |
| C4 | IO2 | I/O | Data Input Output 2 |
| D2 | SO (IO1) | I/O | Data Output (Data Input Output 1) |
| D3 | SI (IO0) | I/O | Data Input (Data Input Output 0) |
| D4 | IO3 | I/O | Data Input Output 3 |

**Table 3. Pin Description for WSON8 package**

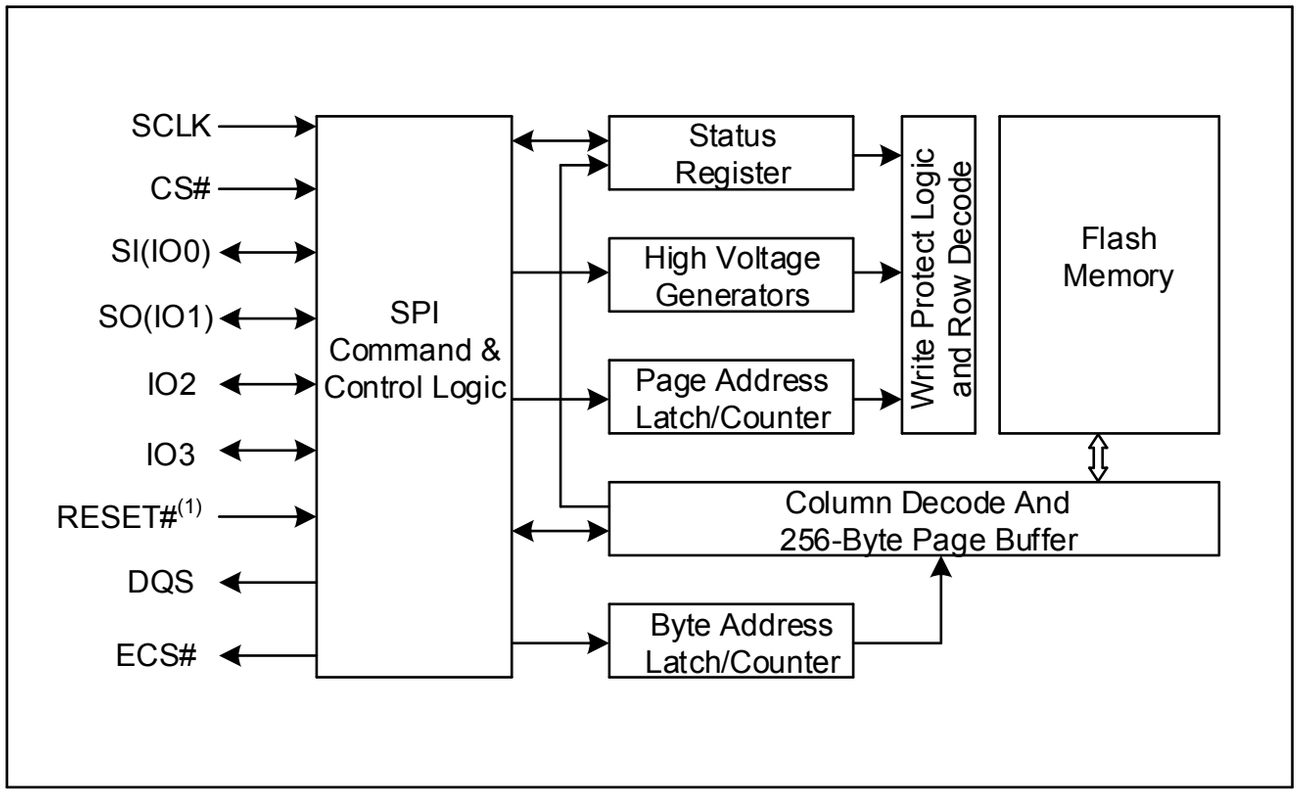
| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | CS# | I | Chip Select Input |
| 2 | SO (IO1) | I/O | Data Output (Data Input Output 1) |
| 3 | IO2 | I/O | Data Input Output 2 |
| 4 | VSS | | Ground |
| 5 | SI (IO0) | I/O | Data Input (Data Input Output 0) |
| 6 | SCLK | I | Serial Clock Input |
| 7 | IO3 | I/O | Data Input Output 3 |
| 8 | VCC | | Power Supply |

Note:

1. Only for special order, Pin 3 of 16-LEAD SOP package or Pin A4 of 24-BALL TFBGA (5x5 ball array) package is RESET# pin. Please contact GigaDevice for detail

## BLOCK DIAGRAM

**Figure 2 Block Diagram**




Note:

1. Only for special order, Pin 3 of 16-LEAD SOP package or Pin A4 of 24-BALL TFBGA (5x5 ball array) package is RESET# pin. Please contact GigaDevice for detail

# 3. MEMORY ORGANIZATION

**GD25B257D**

| Each device has | Each block has | Each sector has | Each page has | |
|---|---|---|---|---|
| 32M | 64/32K | 4K | 256 | Bytes |
| 128K | 256/128 | 16 | - | pages |
| 8192 | 16/8 | - | - | sectors |
| 512/1024 | - | - | - | blocks |

**UNIFORM BLOCK SECTOR ARCHITECTURE**

**GD25B257D**

**Table 4. GD25B257D 64K Bytes Block Sector Architecture**

| Block | Sector | Address Range | |
|---|---|---|---|
| 511 | 8191 | 01FF F000H | 01FF FFFFH |
| | ..... | ..... | ..... |
| | 8176 | 01FF 0000H | 01FF 0FFFH |
| 510 | 8175 | 01FE F000H | 01FE FFFFH |
| | ..... | ..... | ..... |
| | 8160 | 01FE 0000H | 01FE 0FFFH |
| 509 | 8159 | 01FD F000H | 01FD FFFFH |
| | ..... | ..... | ..... |
| | 8144 | 01FD 0000H | 01FD 0FFFH |
| ..... | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| ..... | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| | ..... | ..... | ..... |
| 2 | 47 | 0002 F000H | 0002 FFFFH |
| | ..... | ..... | ..... |
| | 32 | 0002 0000H | 0002 0FFFH |
| 1 | 31 | 0001 F000H | 0001 FFFFH |
| | ..... | ..... | ..... |
| | 16 | 0001 0000H | 0001 0FFFH |
| 0 | 15 | 0000 F000H | 0000 FFFFH |
| | ..... | ..... | ..... |
| | 0 | 0000 0000H | 0000 0FFFH |

# 4. DEVICE OPERATION

## 4.1. SPI Mode

**Standard SPI**

The GD25B257D features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

**Dual SPI**

The GD25B257D supports Dual SPI operation when using the “Dual Output Fast Read”, “Dual Output Fast Read with 4-Byte address”, “Dual I/O Fast Read” and “Dual I/O Fast Read with 4-Byte address” commands (3BH 3CH BBH and BCH). These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

**Quad SPI**

The GD25B257D supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad Output Fast Read with 4-Byte address”, “Quad I/O Fast Read”, “Quad I/O Fast Read with 4-Byte address” (6BH, 6CH, EBH and ECH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins. For GD25B257D, QE bit is set to 1 as default and cannot be changed.

**DTR Quad SPI**

The GD25B257D supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” (EDH and EEH) command.

These command allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins.

## 4.2. ECC Function

The ECC Correction Signal (ECS#) pin is provided to the system hardware designers to determine the ECC status during any Read operation. When the internal ECC engine is disabled (ECC=0 in Status Register), the ECS# pin is also disabled. When ECC is enabled (ECC=1 in Status Register), the ECS# pin will be pulled low during any 8-Byte Read data output period in which an ECC event has occurred. Depending on the ECS bit setting in the Extended Register, ECS# pin can be used to represent either SEC (Single Error Correction) or DED (Double Error Detection). ECC Correction Signal (ECS#) pin is an Open-Drain connection.

# 5. DATA PROTECTION

The GD25B257D provides the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  -Power-Up/Software Reset (66H+99H)
  -Write Disable (WRDI)
  -Write Status Register (WRSR)
  -Page Program (PP)
  -Quad Page Program (QPP)
  -Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode:
  -The Block Protect (BP3, BP2, BP1, and BP0) bits and Top Bottom (TB) bit define the section of the memory array that can be read but cannot be changed.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66H+99H).

**Table 5. GD25B257D Protected area size**

| Status Register Content | | | | | Memory Content | | | |
|---|---|---|---|---|---|---|---|---|
| TB | BP3 | BP2 | BP1 | BP0 | Blocks | Addresses | Density | Portion |
| X | 0 | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 511 | 01FF0000h-01FFFFFFh | 64KB | Upper 1/512 |
| 0 | 0 | 0 | 1 | 0 | 510 to 511 | 01FE0000h-01FFFFFFh | 128KB | Upper 1/256 |
| 0 | 0 | 0 | 1 | 1 | 508 to 511 | 01FC0000h-01FFFFFFh | 256KB | Upper 1/128 |
| 0 | 0 | 1 | 0 | 0 | 504 to 511 | 01F80000h-01FFFFFFh | 512KB | Upper 1/64 |
| 0 | 0 | 1 | 0 | 1 | 496 to 511 | 01F00000h-01FFFFFFh | 1MB | Upper 1/32 |
| 0 | 0 | 1 | 1 | 0 | 480 to 511 | 01E00000h-01FFFFFFh | 2MB | Upper 1/16 |
| 0 | 0 | 1 | 1 | 1 | 448 to 511 | 01C00000h-01FFFFFFh | 4MB | Upper 1/8 |
| 0 | 1 | 0 | 0 | 0 | 384 to 511 | 01800000h-01FFFFFFh | 8MB | Upper 1/4 |
| 0 | 1 | 0 | 0 | 1 | 256 to 511 | 01000000h-01FFFFFFh | 16MB | Upper 1/2 |
| 1 | 0 | 0 | 0 | 1 | 0 | 00000000h-0000FFFFh | 64KB | Lower 1/512 |
| 1 | 0 | 0 | 1 | 0 | 0 to 1 | 00000000h-0001FFFFh | 128KB | Lower 1/256 |
| 1 | 0 | 0 | 1 | 1 | 0 to 3 | 00000000h-0003FFFFh | 256KB | Lower 1/128 |
| 1 | 0 | 1 | 0 | 0 | 0 to 7 | 00000000h-0007FFFFh | 512KB | Lower 1/64 |
| 1 | 0 | 1 | 0 | 1 | 0 to 15 | 00000000h-000FFFFFh | 1MB | Lower 1/32 |
| 1 | 0 | 1 | 1 | 0 | 0 to 31 | 00000000h-001FFFFFh | 2MB | Lower 1/16 |
| 1 | 0 | 1 | 1 | 1 | 0 to 63 | 00000000h-003FFFFFh | 4MB | Lower 1/8 |
| 1 | 1 | 0 | 0 | 0 | 0 to 127 | 00000000h-007FFFFFh | 8MB | Lower 1/4 |
| 1 | 1 | 0 | 0 | 1 | 0 to 255 | 00000000h-00FFFFFFh | 16MB | Lower 1/2 |
| X | 1 | 1 | 0 | X | ALL | 00000000h-01FFFFFFh | 32MB | ALL |
| X | 1 | X | 1 | X | ALL | 00000000h-01FFFFFFh | 32MB | ALL |

# 6. ECC Operation

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device operation life and improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In GD25B257D, every aligned 8-Byte data (A[2:0] = 0, 0, 0) stored in the memory array will be checked by the internal ECC engine using SEC-DED (Single Error Correction – Double Error Detection) Hsiao Codes algorithm. With 8-Byte ECC data granularity, ECC calculation latency time can be minimized and highest level of data integrity can be preserved.

The default value of all memory data is FFH (Erased) when the device is shipped from the factory. A “Page Program (02H)” or a “Quad Page Program (32H)” command can be used to program the user data into the memory array. When ECC is enabled (ECC=1 in Status Register), ECC calculation will be performed during the internal programming operation and the results are stored in the redundancy or spare area of the memory array. It is necessary to program every page in aligned 8-Byte granularity so that ECC engine can store the correct ECC information. It is also required that every aligned 8-Byte data granularity can only be programmed once to avoid additional ECC calculation in the same granularity resulting incorrect ECC results. A technique previously known as “Incremental Byte/Bit Programming to the same Byte location” cannot be used for GD25B257D when ECC is enabled.

During data read operations, the internal ECC engine will check the ECC results stored in the spare area and apply necessary error correction or error detection to the main array data being read out. It is necessary to check the ECC Status Bits (SEC and DED) in the Extended Register after every Read operation to see if the data read out contains any error or not. A Read operation can start from any Byte address and continue through the entire memory array, so it is not necessary to align the 8-Byte granularity boundary address to start a Read command.

Additional hardware monitoring of the ECC status can also be used to observe the ECC status in real time during any data output. When configured, the ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC or DED events.

# 7. STATUS AND EXTENDED ADDRESS REGISTERS

## 7.1. Status Registers

**Table 6. Status Register-1**

| No. | Name | Description | Note |
|---|---|---|---|
| S0 | WIP | Erase/Write In Progress | Volatile, read only |
| S1 | WEL | Write Enable Latch | Volatile, read only |
| S2 | BP0 | Block Protect Bit | Non-volatile writable |
| S3 | BP1 | Block Protect Bit | Non-volatile writable |
| S4 | BP2 | Block Protect Bit | Non-volatile writable |
| S5 | BP3 | Block Protect Bit | Non-volatile writable |
| S6 | TB | Top/Bottom Protect Bit | Non-volatile writable |
| S7 | Reserved | Reserved | Reserved |

**Table 7. Status Register-2**

| No. | Name | Description | Note |
|---|---|---|---|
| S8 | ADS | Current Address Mode | Volatile, read only |
| S9 | QE | Quad Enable | QE = 1 permanently |
| S10 | SUS2 | Program Suspend | Volatile, read only |
| S11 | LB1 | Security Register Lock Bit | Non-volatile writable (OTP) |
| S12 | LB2 | Security Register Lock Bit | Non-volatile writable (OTP) |
| S13 | LB3 | Security Register Lock Bit | Non-volatile writable (OTP) |
| S14 | ECC | ECC Enable | Non-volatile writable |
| S15 | SUS1 | Erase Suspend | Volatile, read only |

**Table 8. Status Register-3**

| No. | Name | Description | Note |
|---|---|---|---|
| S16 | LC0 | Latency Code 0 | Non-volatile writable |
| S17 | LC1 | Latency Code 1 | Non-volatile writable |
| S18 | PE | Program Error bit | Volatile, read only |
| S19 | EE | Erase Error bit | Volatile, read only |
| S20 | ADP | Power Up Address Mode | Non-volatile writable |
| S21 | DRV0 | Output Driver Strength | Non-volatile writable |
| S22 | DRV1 | Output Driver Strength | Non-volatile writable |
| S23 | Reserved | Reserved | Reserved |

The status and control bits of the Status Register are as follows:

**WIP bit**

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

**WEL bit**

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

**TB bit**

The Top Bottom (TB) bit is non-volatile (OTP). The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, and BP0), starting from Top or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set to “1”, the protect area will change to Bottom area of the memory device. This bit is written with the Write Status Register (WRSR) command.

**BP3, BP2, BP1, BP0 bits**

The Block Protect (BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP3, BP2, BP1, and BP0) bits are set to 1, the relevant memory area becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed only if none sector or block is protected.

**QE bit**

The Quad Enable (QE) bit is a non-volatile bit in the Status Register that allows Quad operation. The default value of QE bit is 1 and it cannot be changed, so that the IO2 and IO3 pins are enabled all the time.

**LB3, LB2, LB1 bits.**

The LB3, LB2, LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S11, S12, S13) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1 are 0, the security registers are unlocked. The LB3-LB1 bits can be set to 1 individually using the Write Register instruction. The LB3-LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

**ECC bit**

The on chip ECC engine can be enabled or disabled by the ECC bit. When ECC=1, ECC function is enabled for all Program and Read operations to ensure data integrity and improve device reliability. Aligned 8-Byte granularity is required for Program operations, but not for Read operations.

**SUS1, SUS2 bits**

The SUS1 and SUS2 bit are read only bit in the status register (S15 and S10) that are set to 1 after executing an Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS1 to 1,and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bit are cleared to 0 by Program/Erase Resume (7AH) command, software reset (66H+99H) command as well as a power-down, power-up cycle.

**LC1, LC0 bits**

The Latency Code (LC) selects the mode and number of dummy cycles between the end of address and the start of read data output for all read commands.

Some read commands send mode bits following the address to indicate that the next command will be of the same

type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction Byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional latency cycles as the SCLK frequency is increased.

The following latency code tables provide different latency settings that are configured by GigaDevice.

**Table 9 Latency Code and DTR Mode Frequency Table**

| LC1, LC0 | Dummy clock cycles | Quad IO DTR Read (MHz) |
|---|---|---|
| 00 | 8 | 70/80R |
| 01 | 8 | 70/80R |
| 10 | 6 | 52 |
| 11 | 6 | 52 |

Note:

1. The default value of latency code is 00.
2. Not 100% tested in production.
3. “R” means VCC range=3.0V~3.6V.

**DRV1, DRV0 bits**

The DRV1&DRV0 bits are used to determine the output driver strength for the Read operations.

**Table 10. Driver Strength for Read Operations**

| DRV1,DRV0 | Driver Strength |
|---|---|
| 00 | 100% |
| 01 | 75% (Default) |
| 10 | Reserved |
| 11 | Reserved |

**PE bit**

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

**EE bit**

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space.

Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

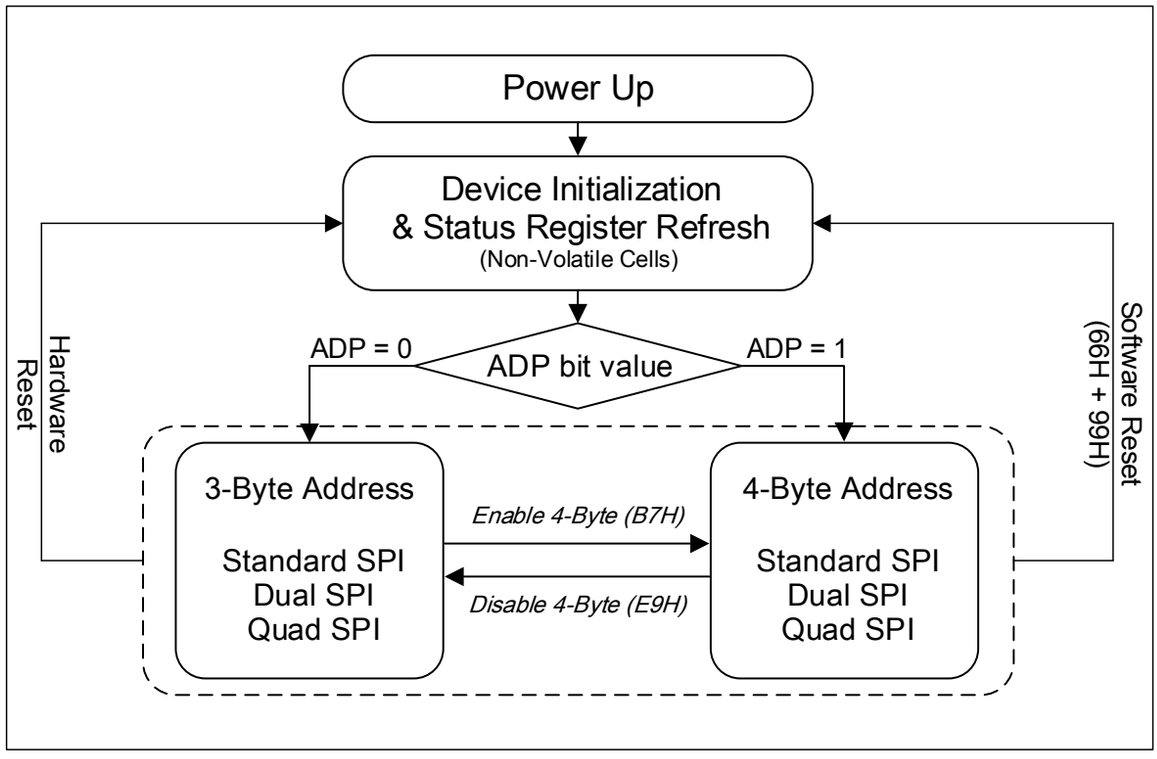
**ADS bit**

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

**ADP bit**

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device

is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0(factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.



## 7.2. Extended Address Register

**Table 11. Extended Address Register**

| No. | Name | Description | Note |
|---|---|---|---|
| EA0 | A24 | Address bit | Volatile writable |
| EA1 | Reserved | Reserved | Reserved |
| EA2 | ECS | ECC Correction Signal bit | Volatile writable |
| EA3 | DLP | Data Learning Pattern Enable bit | Volatile writable |
| EA4 | Reserved | Reserved | Reserved |
| EA5 | Reserved | Reserved | Reserved |
| EA6 | DED | Double Error Detection bit | Volatile, read only |
| EA7 | SEC | Single Error Correction bit | Volatile, read only |

In addition to the Status Registers, GD25B257D provides a volatile Extended Register which consists of the configuration bits for advanced features and the MSB address bit A24. Upon power up or after the execution of a Software/Hardware Reset, the Extended Register values will be cleared to 0. There are two different commands to write the Extended Register. 56H is used to write EA5-EA2 bits, A24 value will not be changed. To change A24 bit setting, C5H should be used, and EA5-EA2 bit values will not be affected.

**A24 bit**

The Extended Address Bit A24 is used only when the device is operating in the 3-Byte Address Mode (ADS=0), which is volatile writable by C5H command. The lower 128Mb memory array (00000000H – 00FFFFFFH) is selected when A24=0, and all instructions with 3-Byte addresses will be executed within that region. When A24=1, the upper 128Mb memory array (01000000H – 01FFFFFFH) will be selected.

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7H)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit A24 setting will be ignored. However, any instruction with 4-Byte address input will replace the Extended Address Bit A24 with new settings.

**SEC, DED bits**

SEC (Single Error Correction) and DED (Double Error Detection) Status Bits are used to show the ECC results for the last Read operation. SEC and DED bits will be cleared to 0 once the device accepts a new Read command.

| SEC, DED | Definitions |
|---|---|
| 00 | No ECC events in all aligned 8-Byte granularities |
| 10 | SEC events in single or multiple 8-Byte granularities, and the data is OK to use. (Unless it contains more than one odd bit errors in 8-Byte granularity) |
| 01 | DED events in single or multiple 8-Byte granularities, and the data contains 2 or more even bit errors. |
| 11 | Both SEC & DED occurred in multiple 8-Byte granularities, and the data contains 2 or more bit errors. |

**DLP bit**

The DLP bit is Data Learning Pattern Enable bit, which is volatile writable by 56H command. For Quad DTR Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, the flash will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output. The Data Learning Pattern can also be defined by a “Write Data Learning Pattern (4AH)” command followed by 8-bit user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its “00110100” default value.

**ECS bit**

The ECS bit is ECC Correction Signal bit, which is volatile writable by 56H command. The hardware ECS# Pin is used by the system to detect ECC events during Read operations when ECC is enabled (ECC=1). When ECS=0, the ECS# Pin will be pulled low during the aligned 8-Byte data output period if there is a SEC (Single Error Correction) event within the 8-Byte ECC granularity. When ECS=1, the ECS# Pin will be pulled low for DED (Double Error Detection) events. When ECC is disabled (ECC=0), the ECS bit value is ignored and ESC# Pin is disabled.

# 8. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-Byte command code must be shifted in to the device, with most significant bit first on SI, and each bit being latched on the rising edges of SCLK.

Every command sequence starts with a one-Byte command code. Depending on the command, this might be followed by address Bytes, or by data Bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a Byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input Byte is not a full Byte, nothing will happen and WEL will not be reset.

When the device is in 3-Byte address mode (ADS=0), please refer to command set in table12 & table13. When the device is in 4-Byte address mode (ADS=1), please refer to command set in table12 & table14.

Extended Address Register setting is effective to achieve A31-A24, accompanying A23-A0 within the instruction, when commands listed in table13 are executed.

Extended Address Register setting is ignored when A31-A24 are given in the instruction listed in table 14 and some specific instruction from table12 (13H, 0CH, 3CH, 6CH, BCH, ECH).

**Table 12. Commands (Standard/Dual/Quad SPI, 3-Byte & 4-Byte address mode)**

| Command Name | Add Mode | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | n-Bytes |
|---|---|---|---|---|---|---|---|---|
| Write Enable | 3 & 4 | 06H | | | | | | |
| Write Disable | 3 & 4 | 04H | | | | | | |
| Volatile SR Write Enable | 3 & 4 | 50H | | | | | | |
| Read Status Register-1 | 3 & 4 | 05H | (S7-S0) | | | | | (cont.) |
| Read Status Register-2 | 3 & 4 | 35H | (S15-S8) | | | | | (cont.) |
| Read Status Register-3 | 3 & 4 | 15H | (S23-S16) | | | | | |
| Write Status Register-1 | 3 & 4 | 01H | S7-S0 | | | | | |
| Write Status Register-1&2 | 3 & 4 | 01H | S7-S0 | S15-S8 | | | | |
| Write Status Register-2 | 3 & 4 | 31H | S15-S8 | | | | | |
| Write Status Register-3 | 3 & 4 | 11H | S23-S16 | | | | | |
| Read Extended Addr. Register | 3 & 4 | C8H | (EA7-EA0) | | | | | |
| Write Extended Addr. Register | 3 & 4 | C5H | EA7-EA0 | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Write Extended Addr. Register | 3 & 4 | 56H | EA7-EA0 | | | | | |
| Write Data Learning Pattern | 3 & 4 | 4AH | P7-P0 | | | | | |
| Chip Erase | 3 & 4 | C7/60H | | | | | | |
| Enable Reset | 3 & 4 | 66H | | | | | | |
| Reset | 3 & 4 | 99H | | | | | | |
| Program/Erase Suspend | 3 & 4 | 75H | | | | | | |
| Program/Erase Resume | 3 & 4 | 7AH | | | | | | |
| Set Burst with Wrap (5) | 3 & 4 | 77H | dummy W7-W0 | | | | | |
| Release From Deep Power-Down | 3 & 4 | ABH | | | | | | |
| Read Device ID | 3 & 4 | ABH | dummy | dummy | dummy | (DID7-DID0) | | (cont.) |
| Deep Power-Down | 3 & 4 | B9H | | | | | | |
| Manufacturer/ Device ID | 3 & 4 | 90H | 00H | 00H | 00H | (MID7-MID0) | (DID7-DID0) | (cont.) |
| Manufacturer/ Device ID by Dual I/O | 3 & 4 | 92H | A23-A8 | A7-A0, M7-M0 | (MID7-MID0) (DID7-DID0) | | | |
| Manufacturer/ Device ID by Quad I/O | 3 & 4 | 94H | A23-A0, M7-M0 | dummy (5) (MID7-MID0) (DID7-DID0) | | | | |
| Read Identification | 3 & 4 | 9FH | (MID7-MID0) | (JDID15-JDID8) | (JDID7-JDID0) | | | (cont.) |
| Enter 4-Byte Address Mode | 3 & 4 | B7H | | | | | | |
| Exit 4-Byte Address Mode | 3 & 4 | E9H | | | | | | |
| Read Data with 4-Byte Address | 3 & 4 | 13H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | |
| Fast Read with 4-Byte Address | 3 & 4 | 0CH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Fast Read Dual Output with 4-Byte Address (1) | 3 & 4 | 3CH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Fast Read Quad Output with 4-Byte Address (3) | 3 & 4 | 6CH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Fast Read Dual I/O with 4-Byte Address (2) | 3 & 4 | BCH | A31-A24 A23-A 16 | A15-A8 A7-A0 | M7-M0 (D7-D0) | | | |
| Fast Read Quad I/O with 4-Byte Address (4) | 3 & 4 | ECH | A31-A24 A23-A 16 A15-A8 A7-A0 | M7-M0 dummy dummy D7-D0 | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DTR Quad I/O Fast Read with 4-Byte Address | 3 & 4 | EEH | A31-A0<br>M7-M0<br>dummy | dummy<br>(D7-D0)(3) | | | | (cont.) |
| Page Program with 4-Byte Address | 3 & 4 | 12H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | D7-D0 | Next Byte |
| Quad Page Program with 4-Byte Address | 3 & 4 | 34H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | D7-D0 | |
| Sector Erase with 4-Byte Address | 3 & 4 | 21H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase(32K) with 4-Byte Address | 3 & 4 | 5CH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase(64K) with 4-Byte Address | 3 & 4 | DCH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | |
| Clear SR Flags | 3 & 4 | 30H | | | | | | |
| Read Serial Flash Discoverable Parameter | 3 & 4 | 5AH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (cont.) |

**Table 13. Commands (Standard/Dual/Quad SPI, 3-Byte address)**

| Command Name | Add Mode | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | n-Bytes |
|---|---|---|---|---|---|---|---|---|
| Read Data | 3 | 03H | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | (Next Byte) | (cont.) |
| Fast Read | 3 | 0BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (cont.) |
| Dual Output Fast Read (1) | 3 | 3BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(1) | (cont.) |
| Dual I/O Fast Read (2) | 3 | BBH | A23-A8(2) | A7-A0<br>M7-M0(2) | (D7-D0)(1) | | | (cont.) |
| Quad Output Fast Read (3) | 3 | 6BH | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(3) | (cont.) |
| Quad I/O Fast Read (4) | 3 | EBH | A23-A0<br>M7-M0(4) | dummy | (D7-D0)(3) | | | (cont.) |
| DTR Quad I/O Fast Read | 3 | EDH | A23-A0<br>dummy | dummy<br>(D7-D0)(3) | | | | (cont.) |
| Page Program | 3 | 02H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | Next Byte | |
| Quad Page Program | 3 | 32H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | | |
| Sector Erase | 3 | 20H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(32K) | 3 | 52H | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(64K) | 3 | D8H | A23-A16 | A15-A8 | A7-A0 | | | |
| Read Unique ID | 3 | 4BH | dummy | dummy | dummy | dummy | (UID7-UID0) | (cont.) |
| Erase Security Registers (6) | 3 | 44H | A23-A16 | A15-A8 | A7-A0 | | | |
| Program Security | 3 | 42H | A23-A16 | A15-A8 | A7-A0 | D7-D0 | D7-D0 | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Registers (6) | | | | | | | | |
| Read Security Registers (6) | 3 | 48H | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | |

**Table 14. Commands (Standard/Dual/Quad SPI, 4-Byte address)**

| Command Name | Add Mode | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Bytes-7 | n-Bytes |
|---|---|---|---|---|---|---|---|---|---|
| Read Data | 4 | 03H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | | (cont.) |
| Fast Read | 4 | 0BH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (cont.) |
| Dual Output Fast Read (1) | 4 | 3BH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(1) | (cont.) |
| Dual I/O Fast Read (2) | 4 | BBH | A31-A24<br>A23-A16 | A15-A8<br>A7-A0 | M7-M0(2)<br>dummy | (D7-D0)(1) | | | |
| Quad Output Fast Read (3) | 4 | 6BH | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0)(1) | (cont.) |
| Quad I/O Fast Read (4) | 4 | EBH | A31-A24<br>A23-A16<br>A15-A8<br>A7-A0 | M7-M0(4)<br>dummy<br>dummy<br>(D7-D0)(3) | | | | | (cont.) |
| DTR Quad I/O Fast Read | 4 | EDH | A31-A24<br>A23-A16<br>A15-A8<br>A7-A0 | dummy<br>(D7-D0)(3) | | | | | (cont.) |
| Page Program | 4 | 02H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | D7-D0 | D7-D0 | (cont.) |
| Quad Page Program | 4 | 32H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | D7-D0 | | (cont.) |
| Sector Erase | 4 | 20H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(32K) | 4 | 52H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | | |
| Block Erase(64K) | 4 | D8H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | | |
| Read Unique ID | 4 | 4BH | dummy | dummy | dummy | dummy | dummy | (UID7-UID0) | (cont.) |
| Erase Security Registers (6) | 4 | 44H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | | | |
| Program Security Registers (6) | 4 | 42H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | D7-D0 | D7-D0 | (cont.) |
| Read Security Registers (6) | 4 | 48H | A31-A24 | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) | (cont.) |

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8  A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9  A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

   IO0 = (D4, D0, …..)

IO1 = (D5, D1, .....)

IO2 = (D6, D2, .....)

IO3 = (D7, D3,.....)

4. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Address, Continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID

IO0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0, …)

IO1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1, …)

IO2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2, …)

IO3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3, …)

6. Security Registers Address

Security Register1: A23-A16=00H, A15-A12=1H, A11=0b, A10-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A12=2H, A11=0b, A10-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A12=3H, A11=0b, A10-A0= Byte Address.

## Table of ID Definitions:

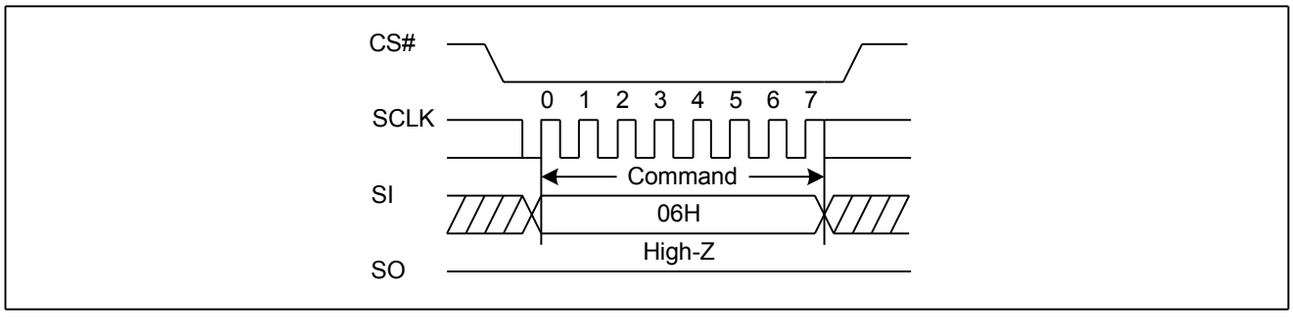
### GD25B257D

| Operation Code | MID7-MID0 | ID15-ID8 | ID7-ID0 |
|---|---|---|---|
| 9FH | C8 | 40 | 19 |
| 90H | C8 | | 18 |
| ABH | | | 18 |

## 8.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR). The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

**Figure 3. Write Enable Sequence Diagram**



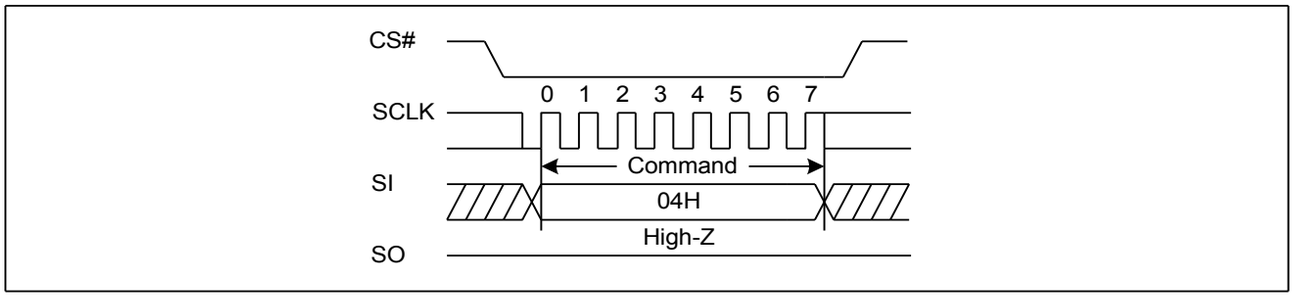

## 8.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit may be set to 0 by issuing the Write Disable (WRDI) command to disable Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), that require WEL be set to 1 for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit =1.

The WEL bit is reset by following condition: Write Disable command (WRDI), Power-up, and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

The Write Disable command sequence: CS# goes low →Sending the Write Disable command →CS# goes high.

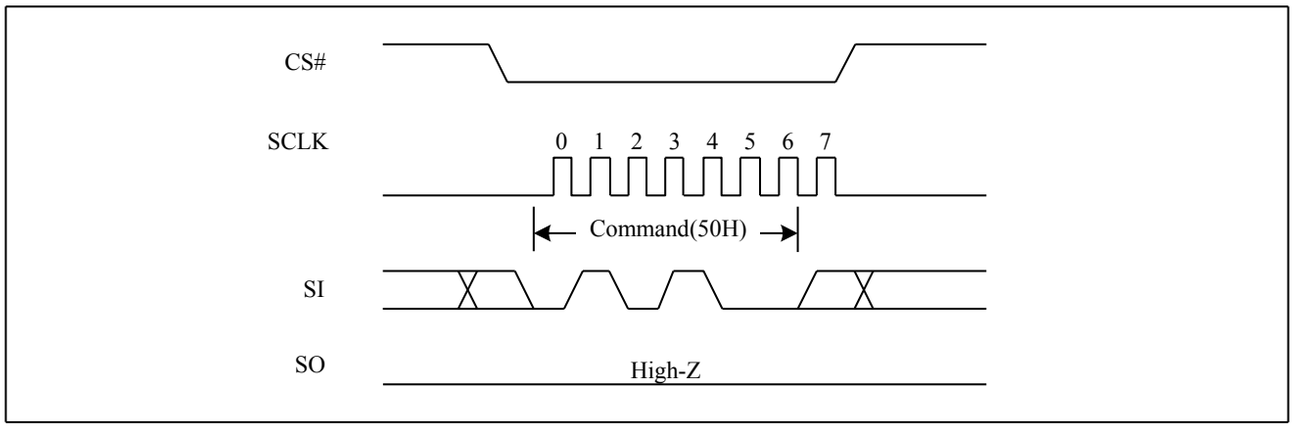
**Figure 4. Write Disable Sequence Diagram**



## 8.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

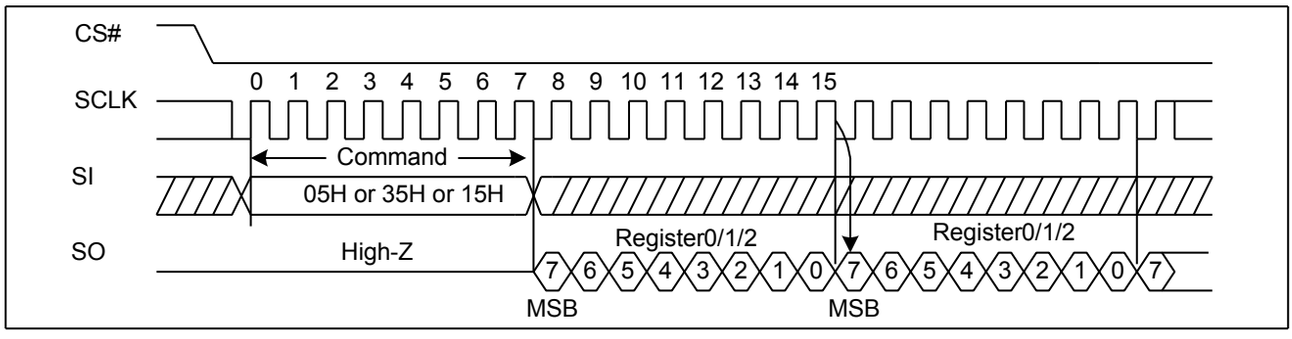
**Figure 5. Write Enable for Volatile Status Register Sequence Diagram**




## 8.4. Read Status Register (RDSR) (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H” / “35H” / “15H”, the SO will output Status Register bits S7~S0 / S15-S8 / S23-S16.

**Figure 6. Read Status Register Sequence Diagram**



## 8.5. Write Status Register (WRSR) (01H or 31H or 11H)

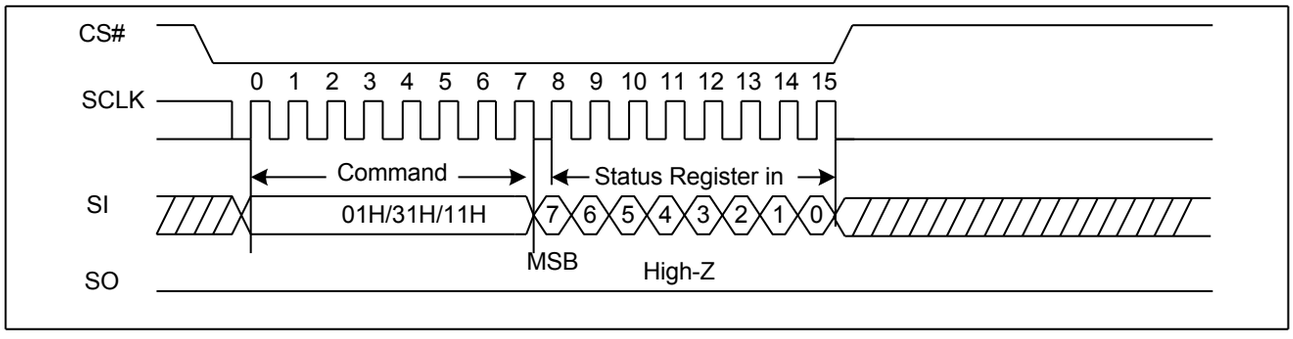
The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S23, S19, S18, S15, S10, S9, S8, S1 and S0 of the Status Register. CS# must be driven high after the eighth of the data Byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is $t_W$) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (TB, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only.

The Write Status Register-1 (01h) command also can write Status Register-1&2. To complete the Write Status Register-1&2 command, the CS# pin must be driven high after the sixteenth bit of data is clocked in. If CS# is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, and the Status Register-2 will not be affected.

**Figure 7. Write Status Register Sequence Diagram**

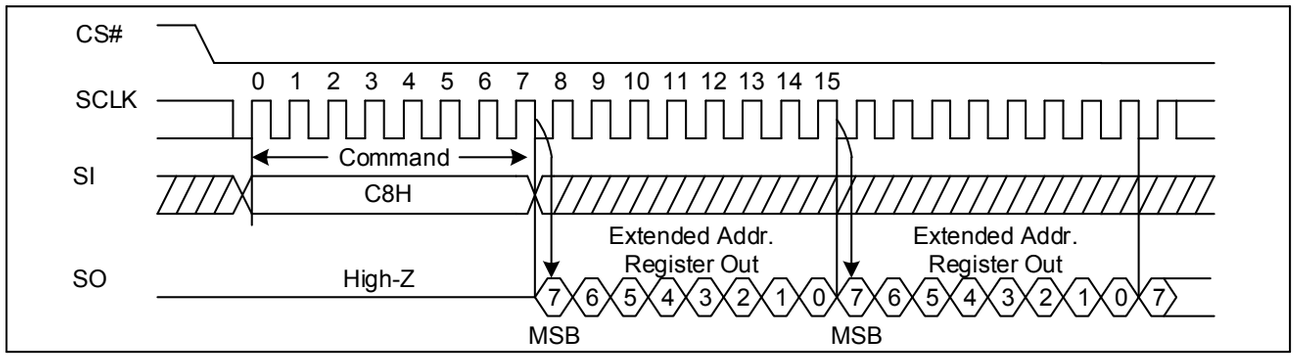


## 8.6. Read Extended Register (C8H)

Extended Register contains ECC Status Bits, several device configuration bits, and Address Bit A24. The Read Extended Register instruction is entered by driving CS# low and shifting the instruction code “C8H” into the SI pin on the rising edge of SCLK. The Extended Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first as shown below.

When the device is in the 4-Byte Address Mode, the value of A24 Bit is not ignored.

**Figure 8 Read Extended Register Sequence Diagram**



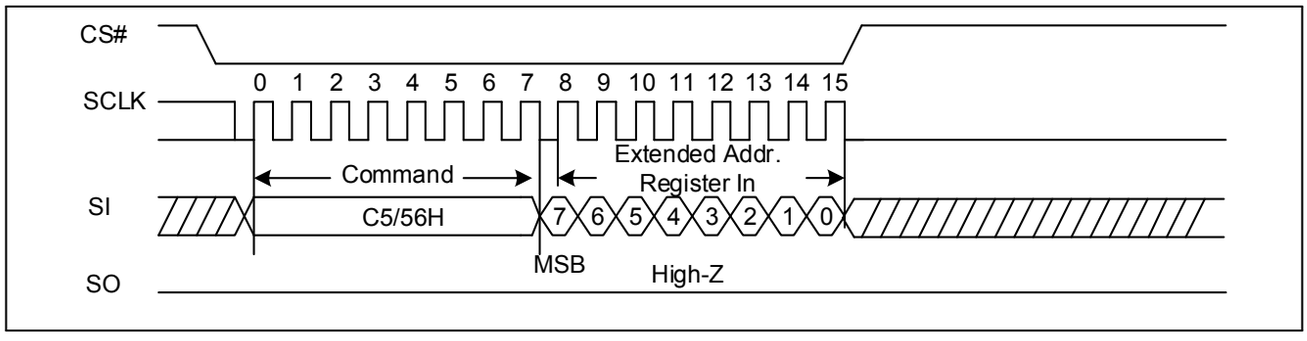

## 8.7. Write Extended Register (C5H or 56H)

The Write Extended Register command could be executed no matter the Write Enable Latch (WEL) bit is 0 or 1. The Write Extended Register instruction is entered by driving CS# low, sending the instruction code “C5/56H”, and then writing the Extended Register data Byte as illustrated below.

C5H is used to write A24 bit in the Extended Register. 56H is used to write EA5-EA2 (DLP, ECS bits).

Upon power up or the execution of a Software/Hardware Reset, the Extended Register bit values will be cleared to 0.

**Figure 9 Write Extended Register Sequence Diagram**



## 8.8. Read Data Bytes (REAC 03H or 4READ 13H)

The Read Data Bytes (READ) command is followed by a 3-Byte address (A23-A0), and each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit being shifted out, at a Max frequency $f_R$, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 10. Read Data Bytes Sequence Diagram (ADS=0)**

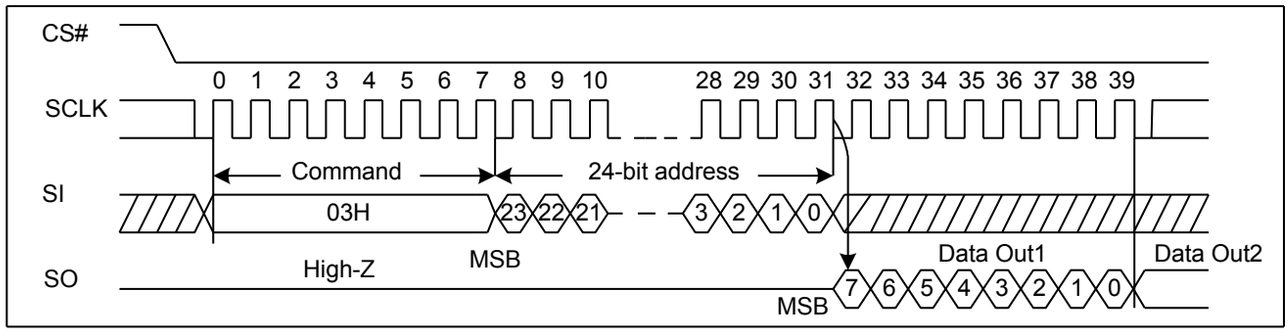



**Figure 11. Read Data Bytes Sequence Diagram (ADS=1)**

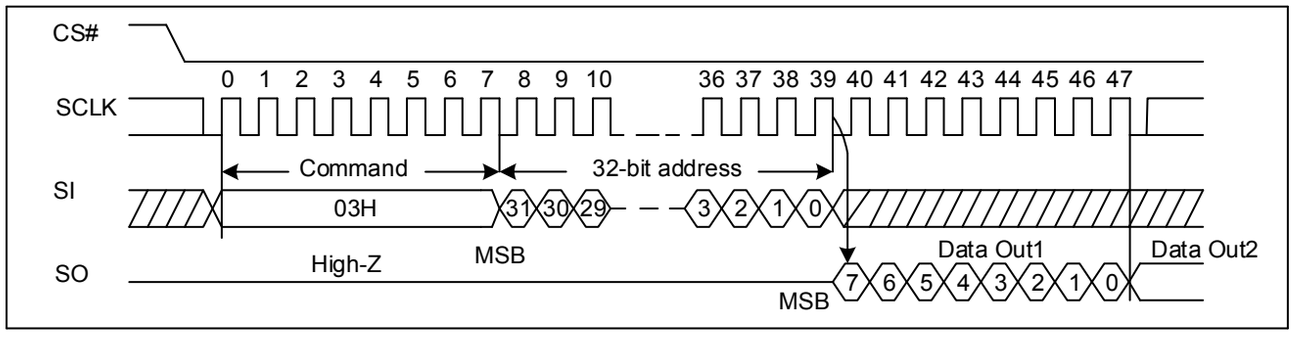
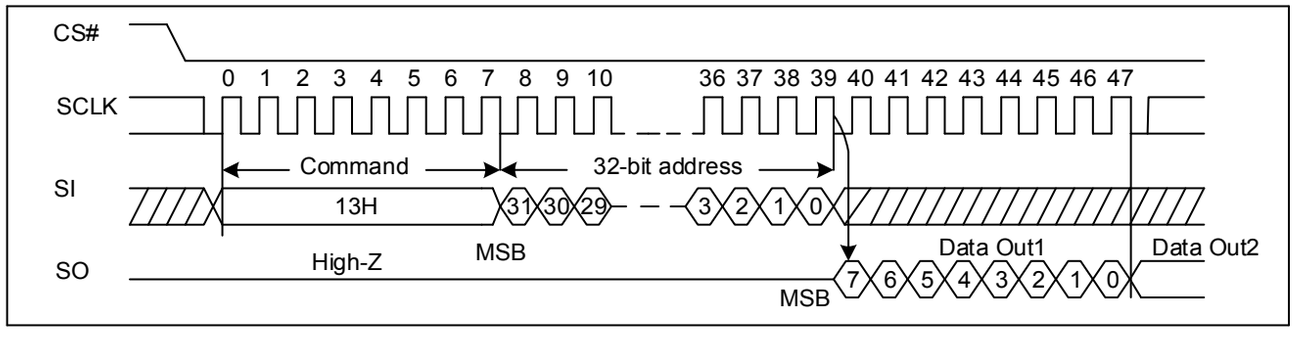



**Figure 12. Read Data with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.9. Read Data Bytes at Higher Speed (Fast Read 0BH or 4Fast Read 0CH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-Byte address (A23-A0) and a dummy Byte, and each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit being shifted out, at a Max frequency $f_C$, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

**Figure 13. Read Data Bytes at Higher Speed Sequence Diagram (ADS=0)**

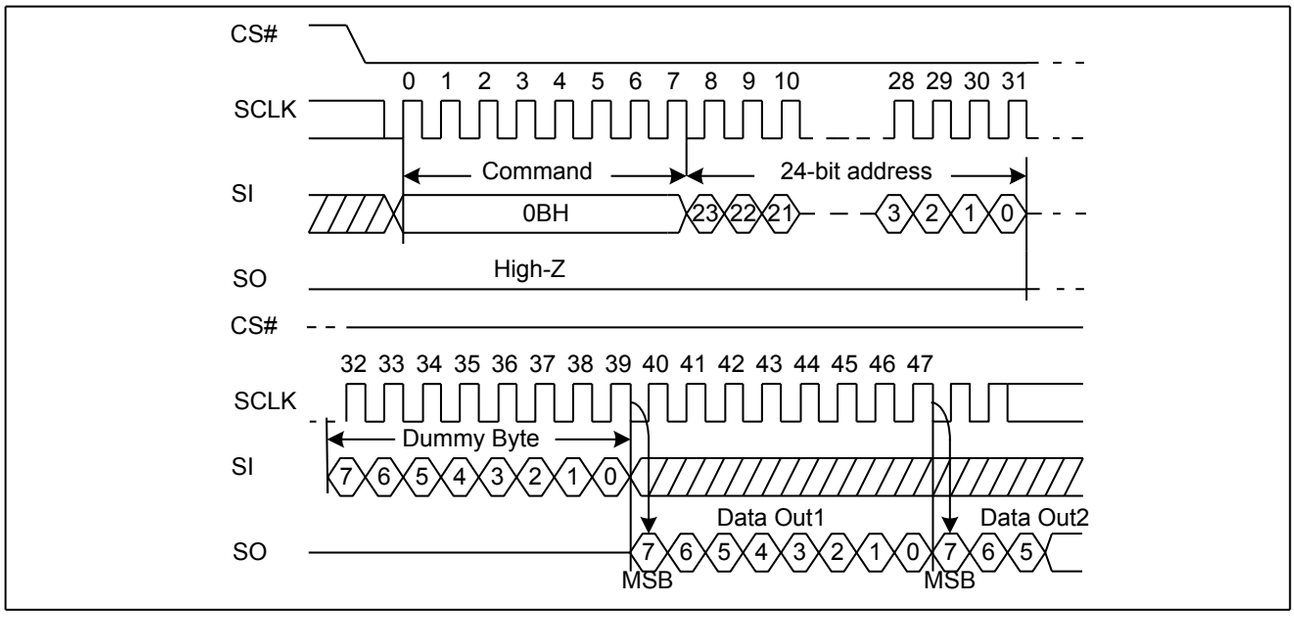



**Figure 14. Read Data Bytes at Higher Speed Sequence Diagram (ADS=1)**

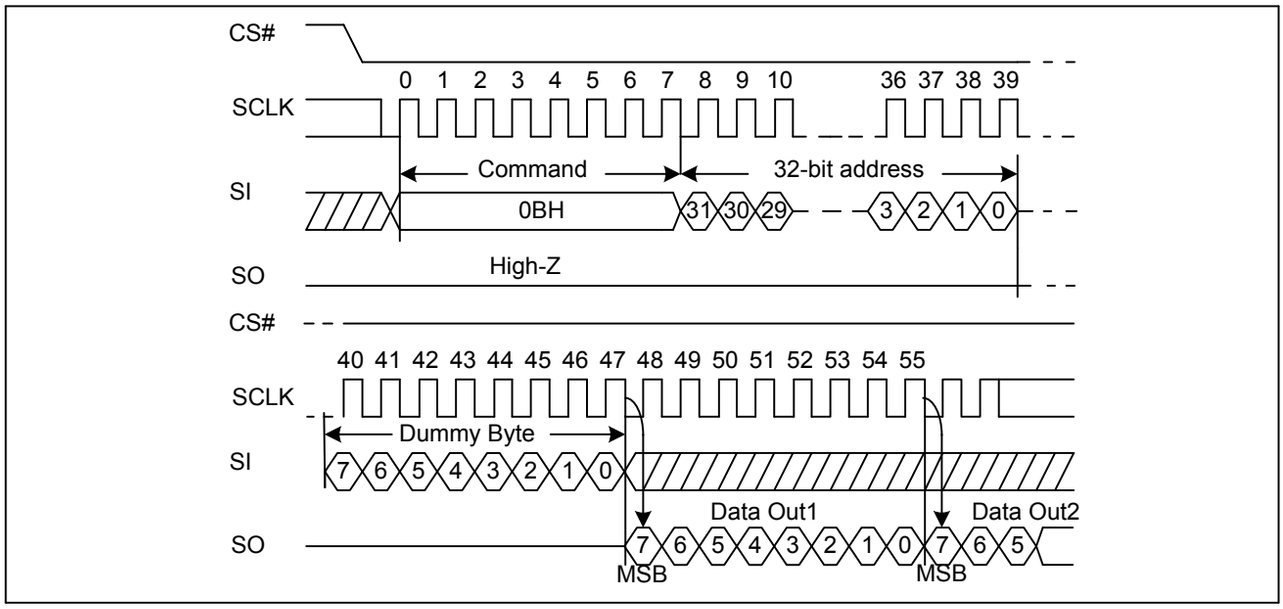
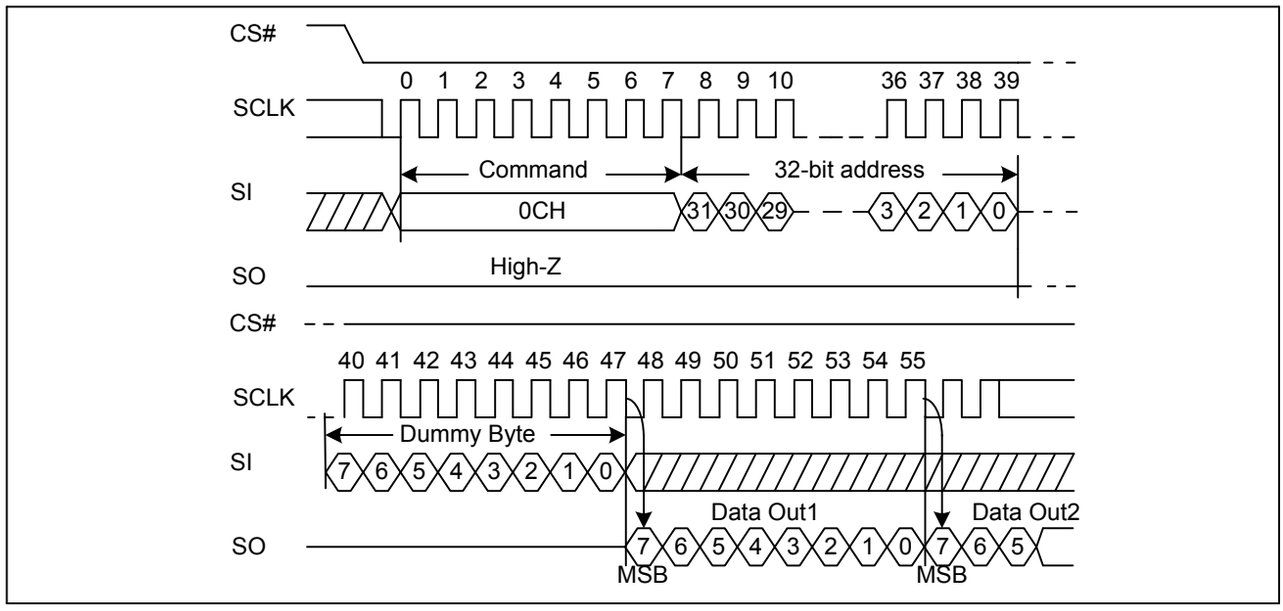


**Figure 15. Fast Read with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**




## 8.10. Dual Output Fast Read (DOFR 3BH or 4DOFR 3CH)

The Dual Output Fast Read command is followed by 3-Byte address (A23-A0) and a dummy Byte, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown below. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

**Figure 16. Dual Output Fast Read Sequence Diagram (ADS=0)**

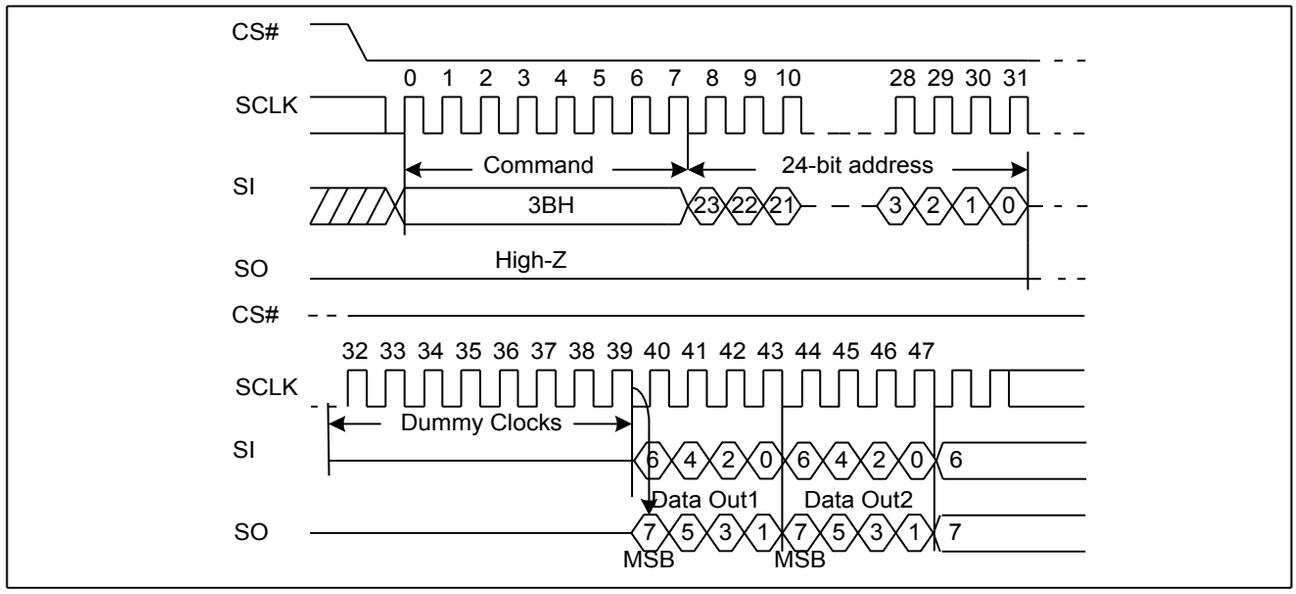


**Figure 17. Dual Output Fast Read Sequence Diagram (ADS=1)**

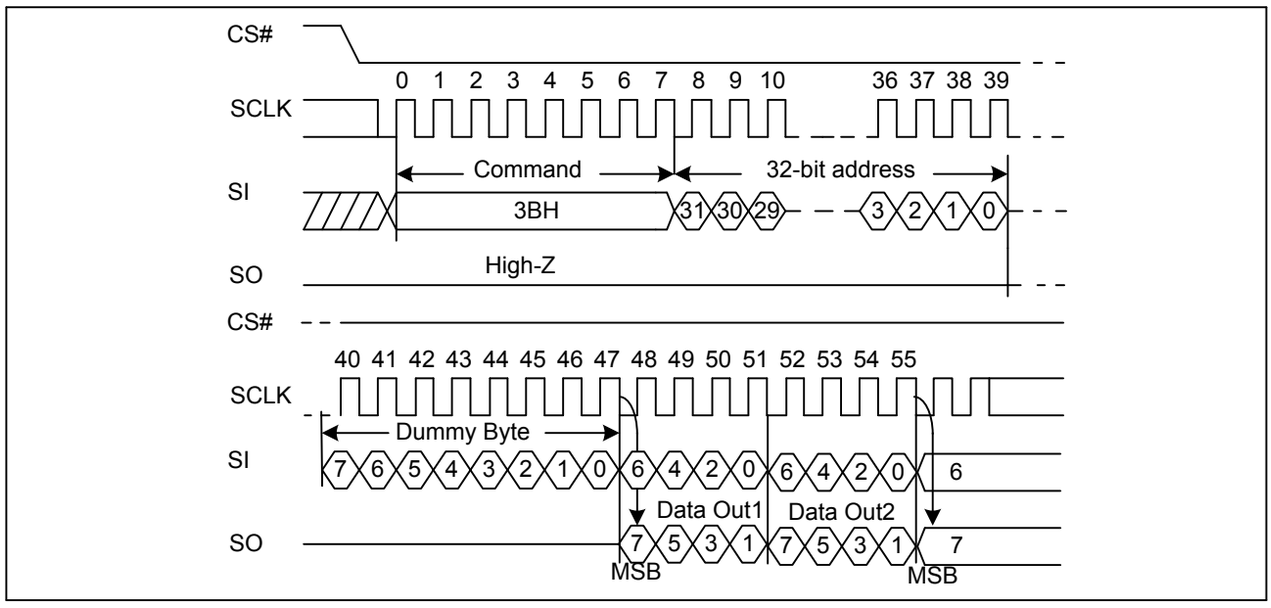
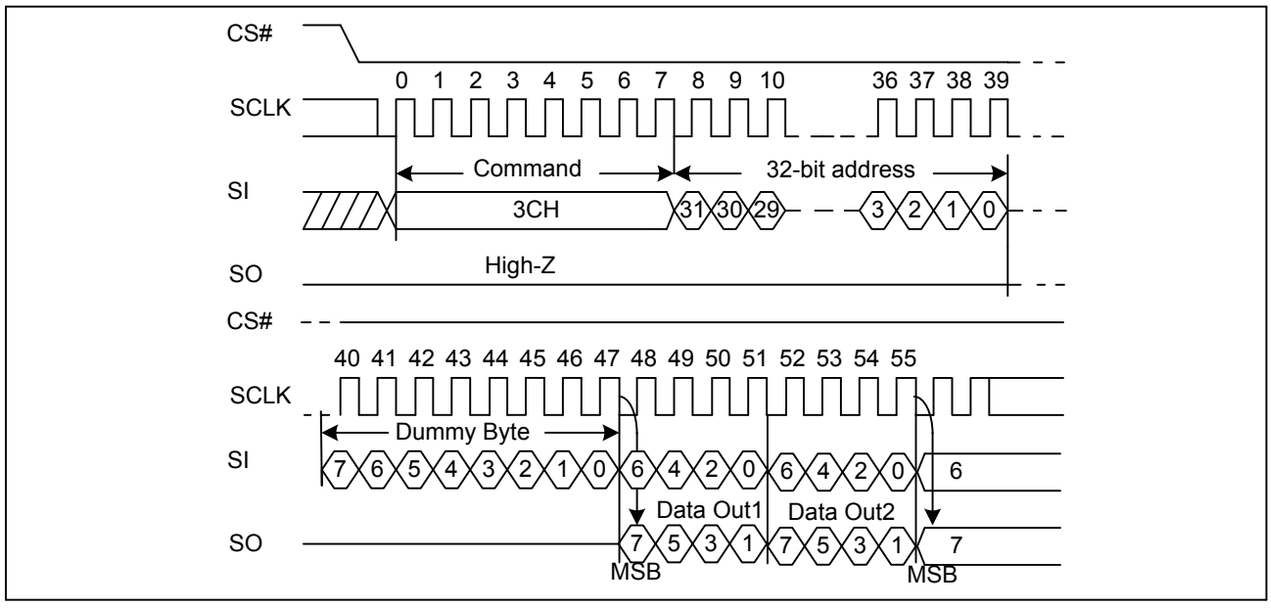



**Figure 18. Dual Output Fast Read with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.11. Quad Output Fast Read (QOFR 6BH or 4QOFR 6CH)

The Quad Output Fast Read command is followed by 3-Byte address (A23-A0) and a dummy Byte, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown below. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

**Figure 19. Quad Output Fast Read Sequence Diagram (ADS=0)**

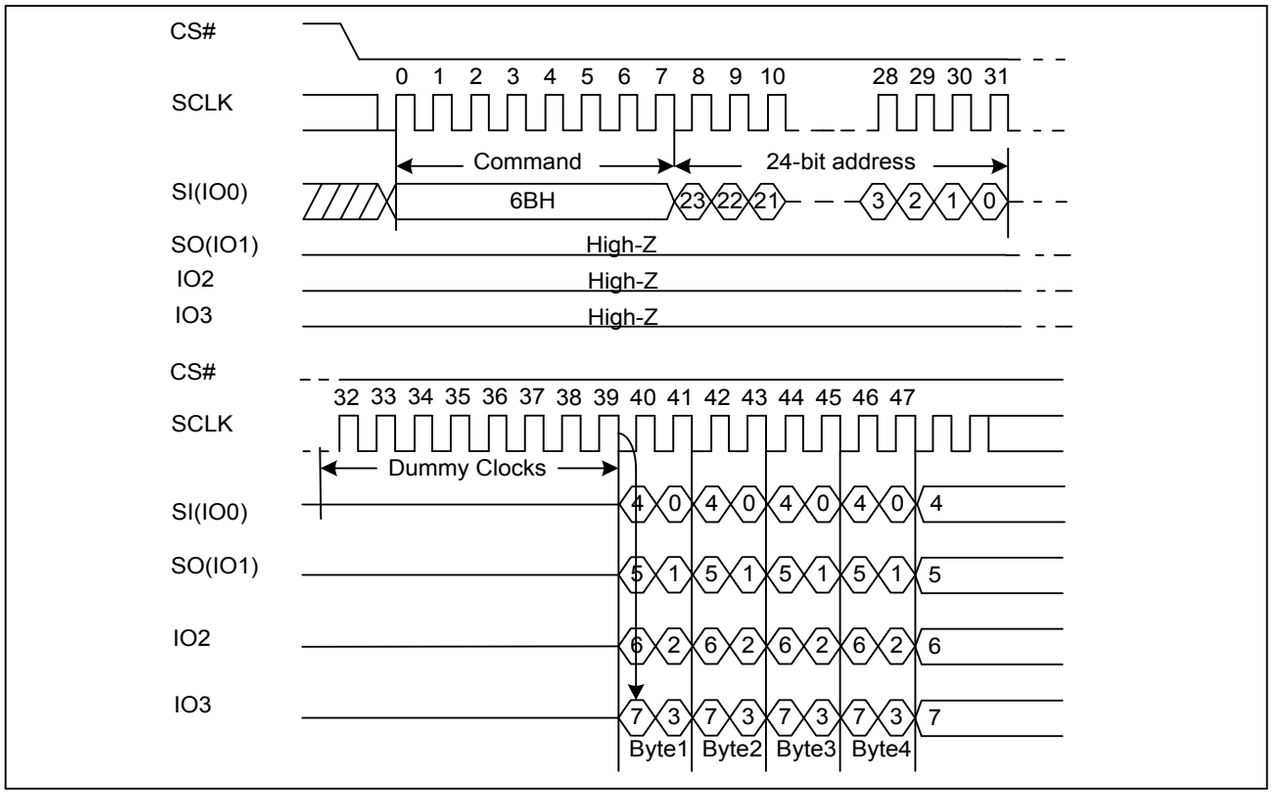


**Figure 20. Quad Output Fast Read Sequence Diagram (ADS=1)**

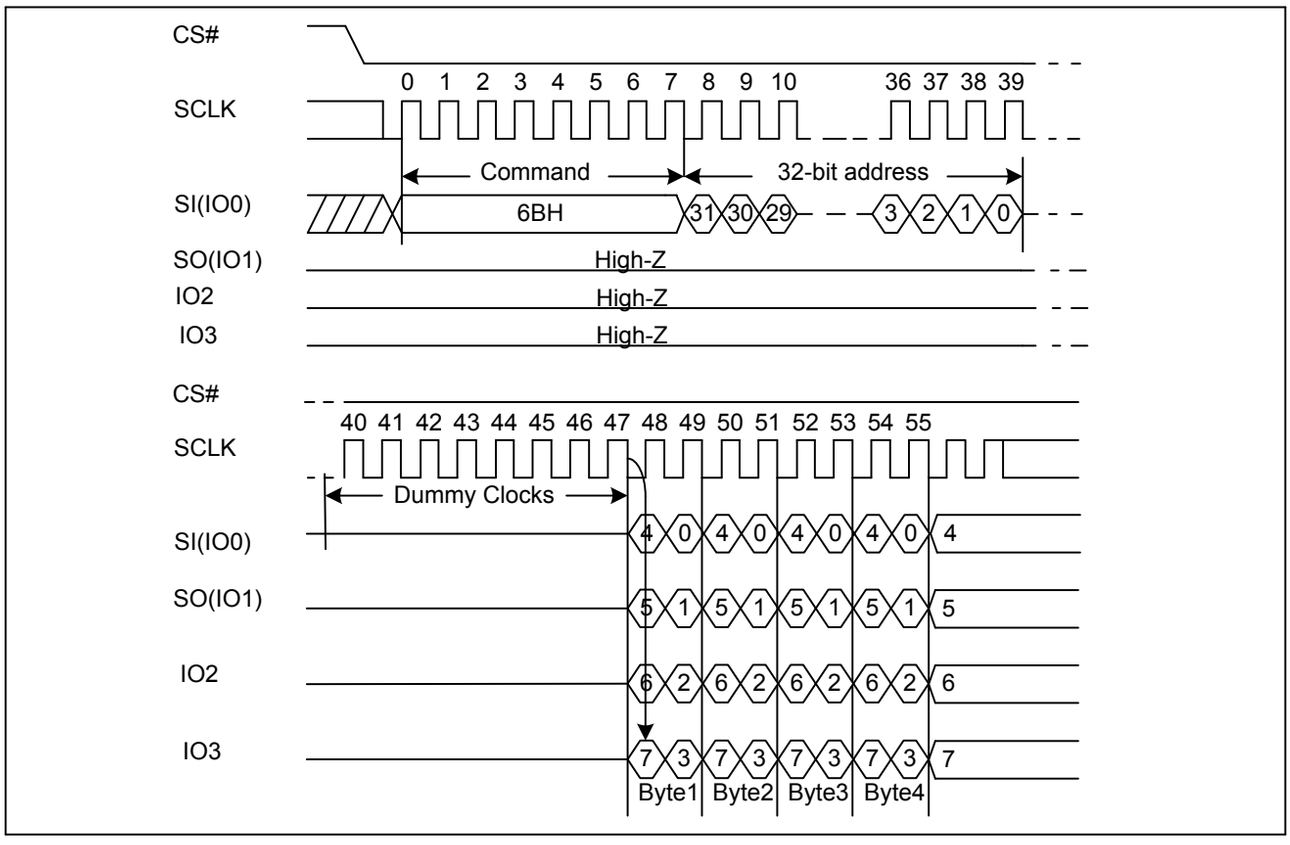
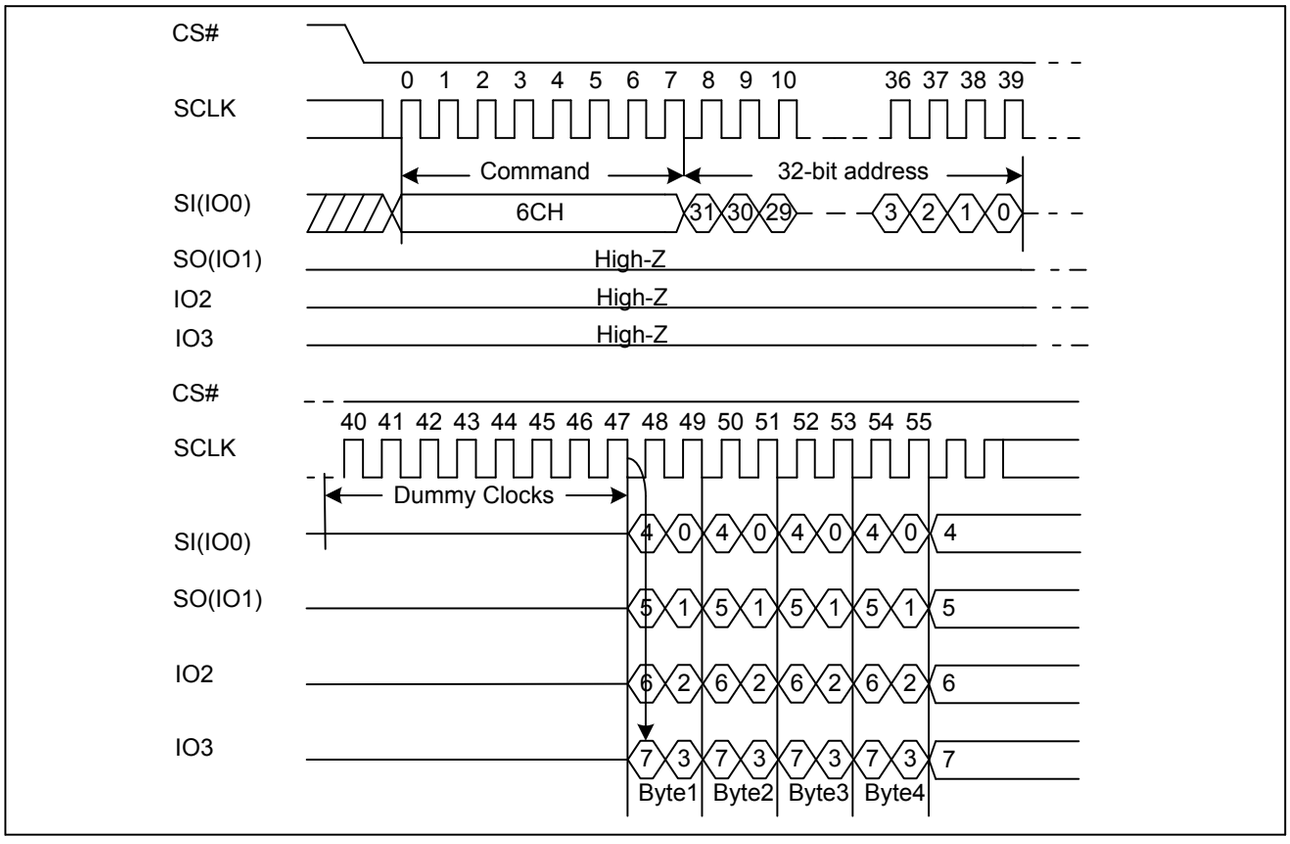


**Figure 21.Fast Read Quad Output with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.12. Dual I/O Fast Read (DIOFR BBH or 4DIOFR BCH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-Byte address (A23-0) and a "Continuous Read Mode" Byte 2-bit per clock by SI and SO, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown below. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

### Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-4) after the input 3-Byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown below. If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command.

**Figure 22. Dual I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=0)**

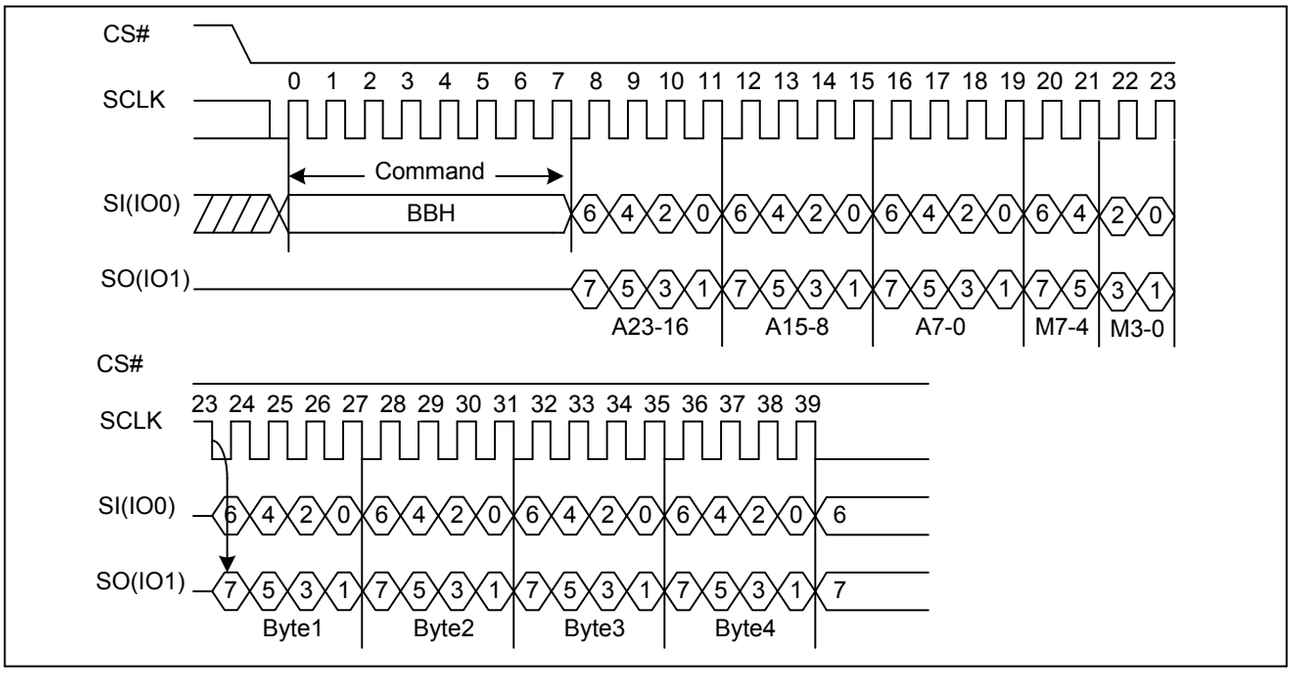


**Figure 23. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=0)**

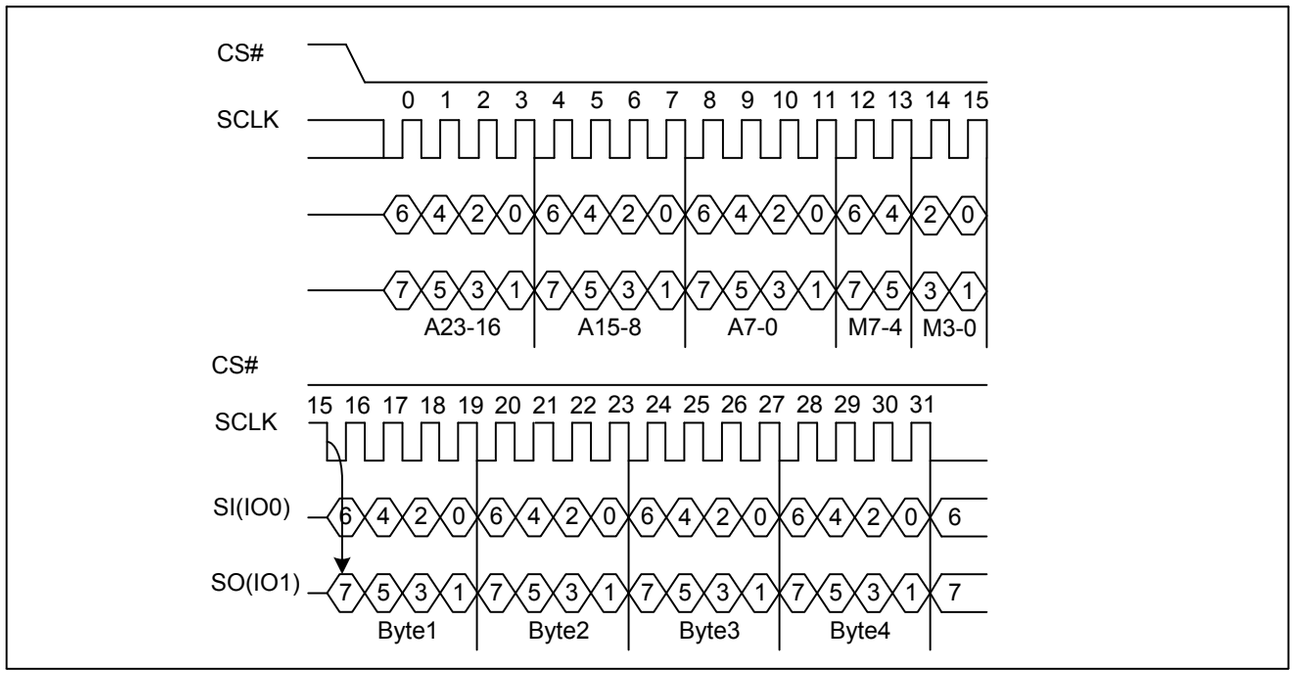



**Figure 24.Dual I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=1)**

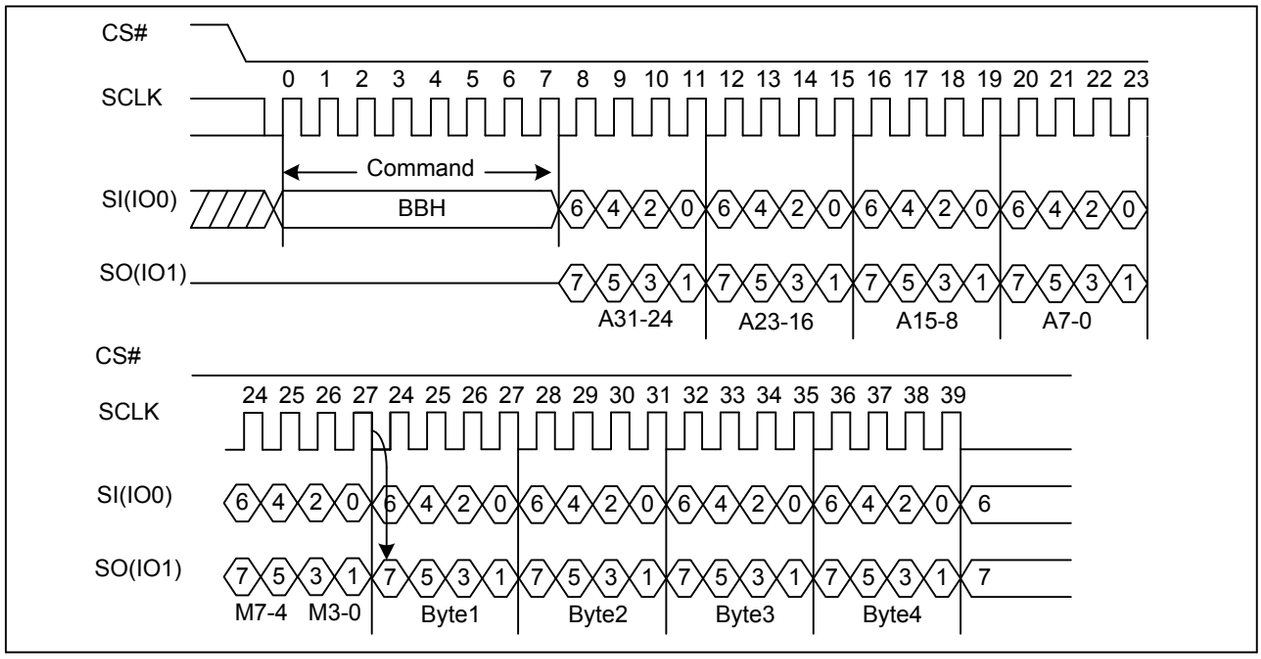


**Figure 25. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0) ADS=1)**

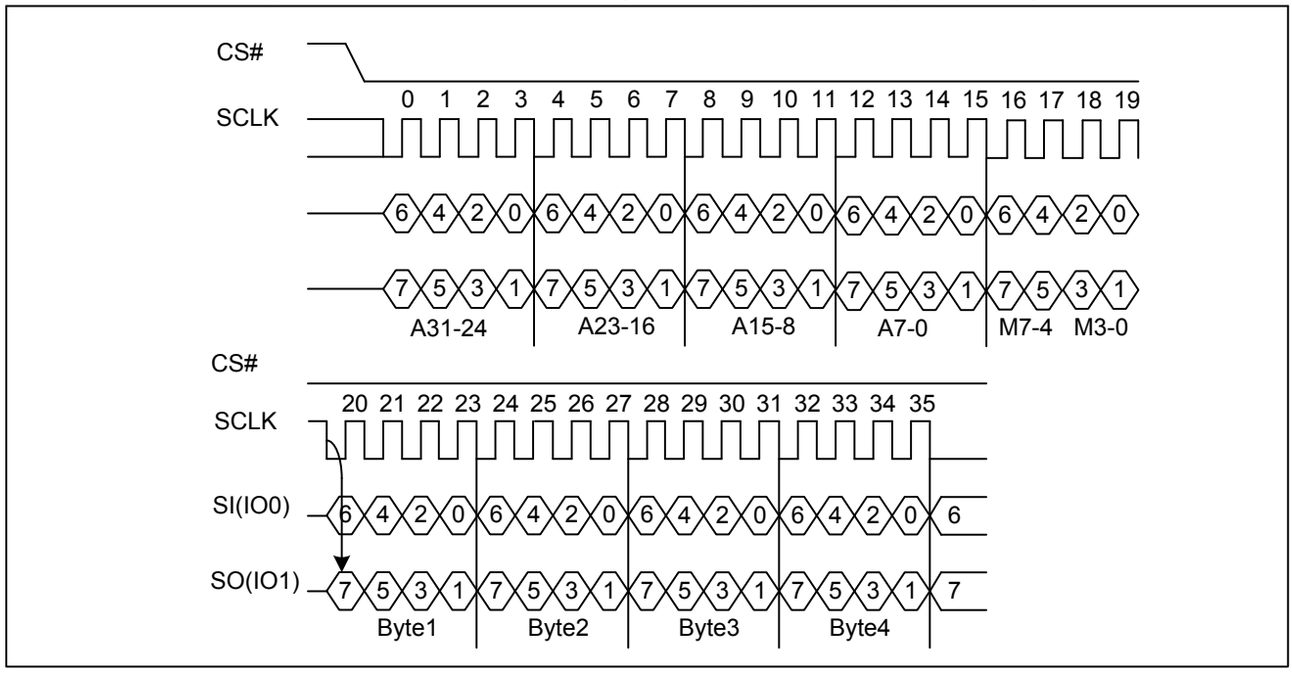



**Figure 26. Dual I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4≠ (1, 0), ADS=0 or ADS=1)**

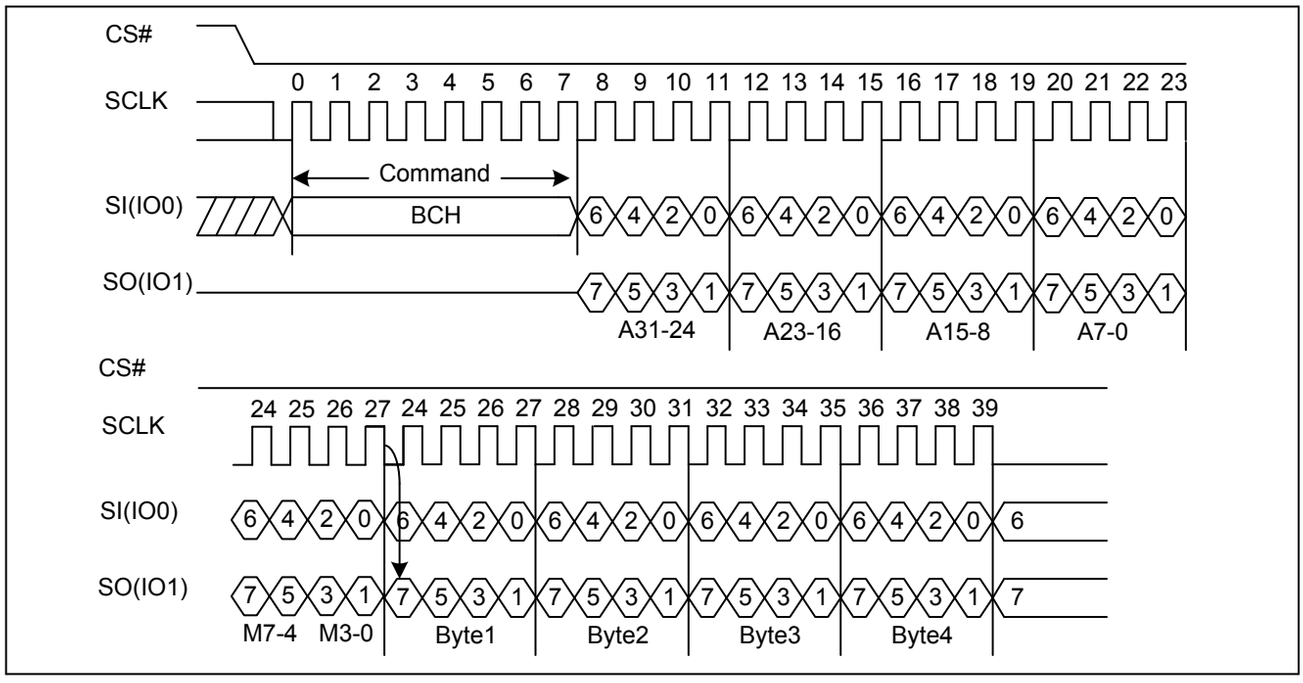
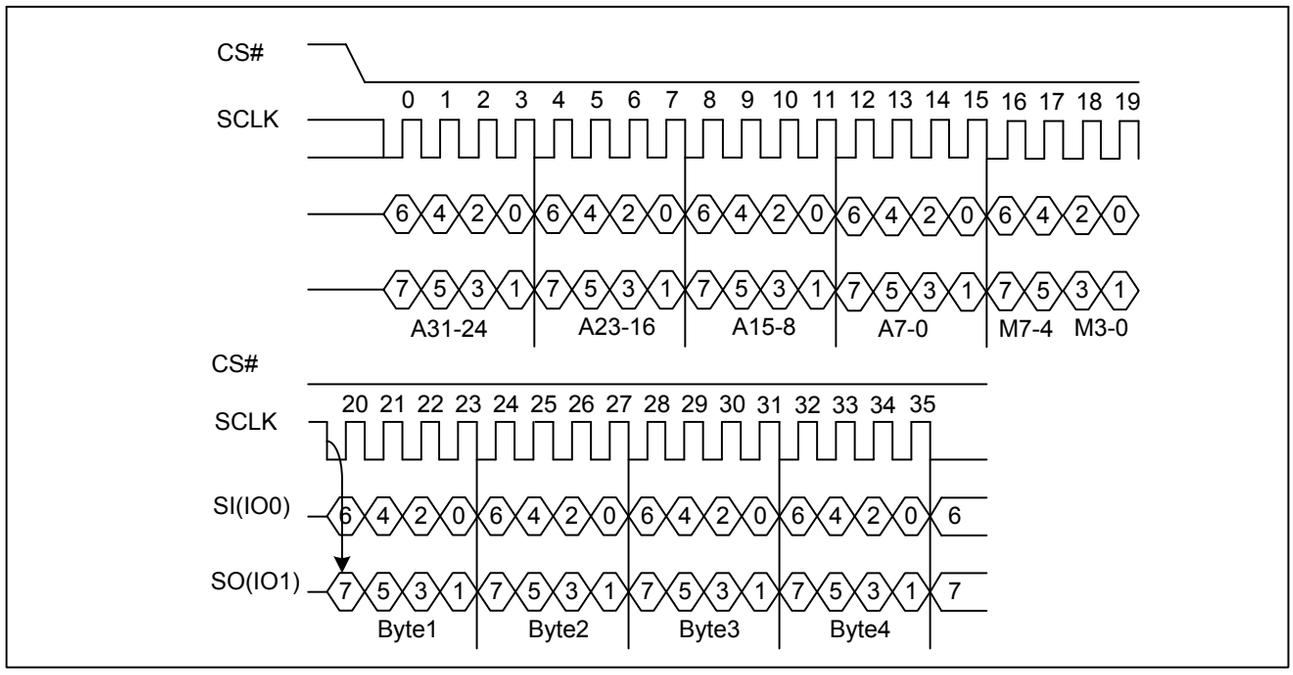


**Figure 27. Dual I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4= (1, 0) ADS=0 or ADS=1)**



## 8.13. Quad I/O Fast Read (QIOFR EBH or 4QIOFR ECH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-Byte address (A23-0) and a "Continuous Read Mode" Byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, and each bit being latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

### Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-Byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command.

**Figure 28. Quad I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=0)**

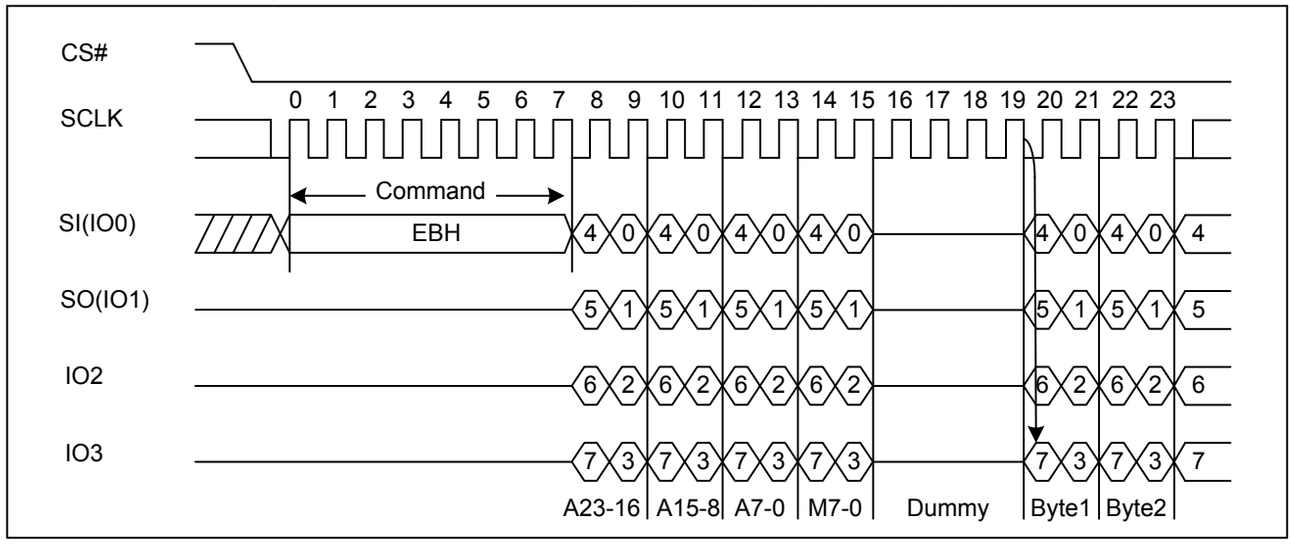



**Figure 29. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=0)**

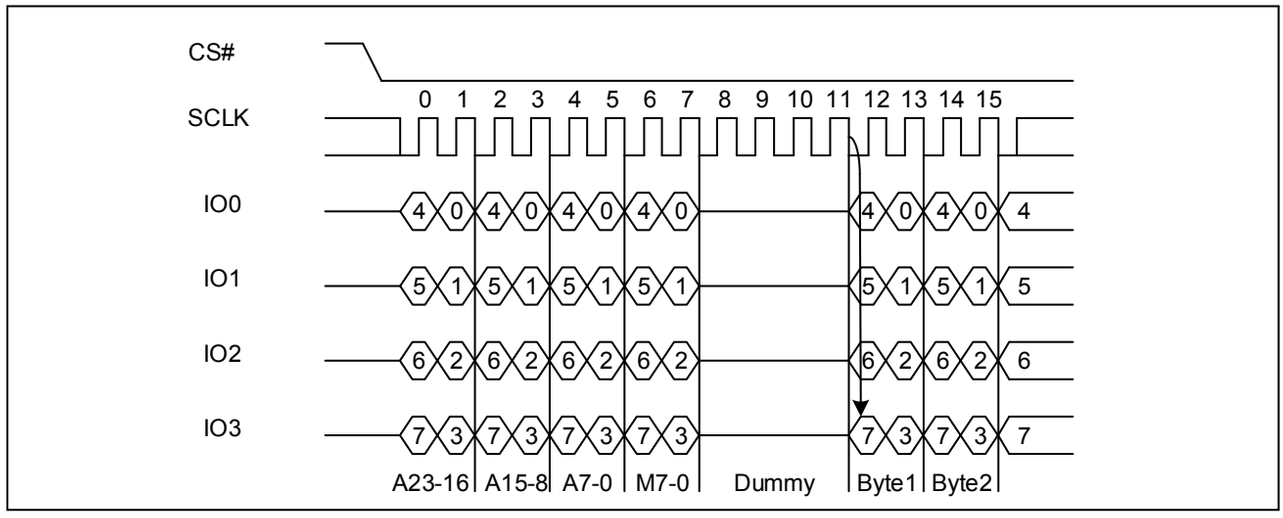


**Figure 30. Quad I/O Fast Read Sequence Diagram (M5-4≠ (1, 0), ADS=1)**

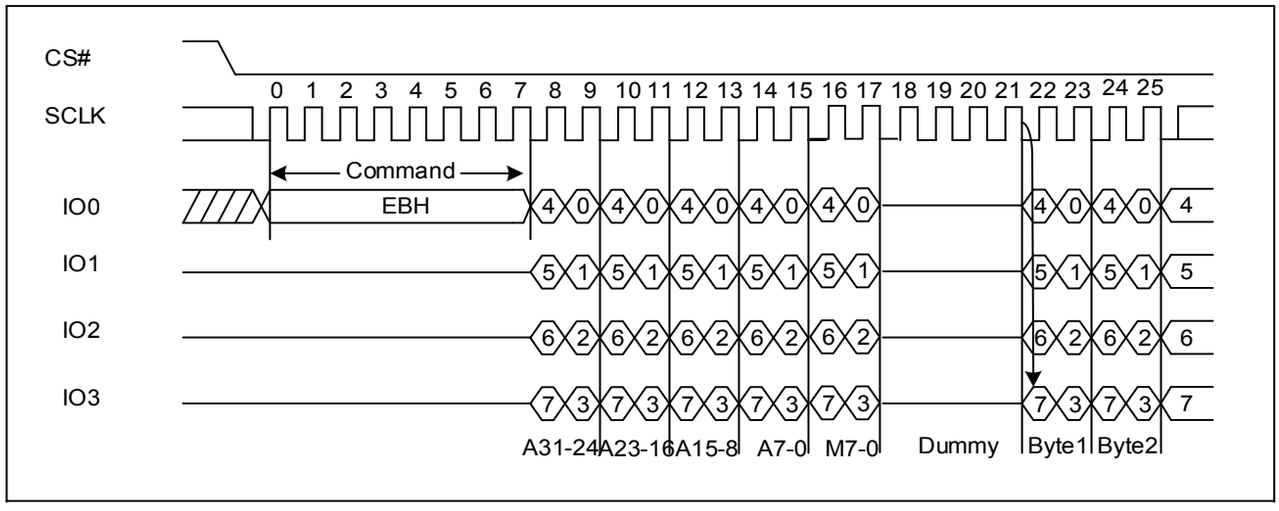



**Figure 31.Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0), ADS=1)**

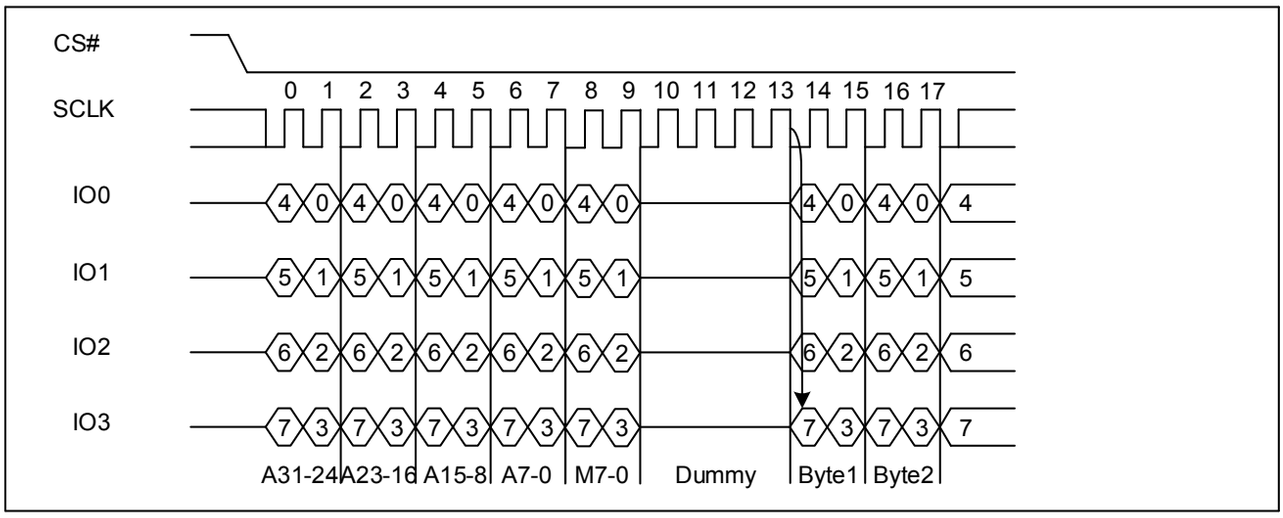



**Figure 32. Quad I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4≠ (1, 0), ADS=0 or ADS=1)**

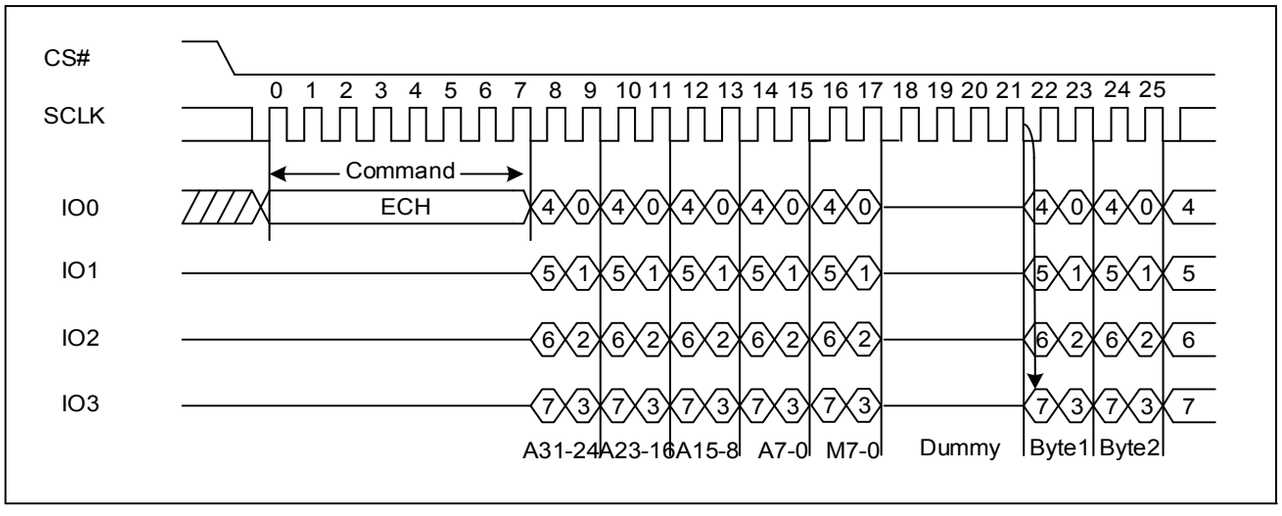
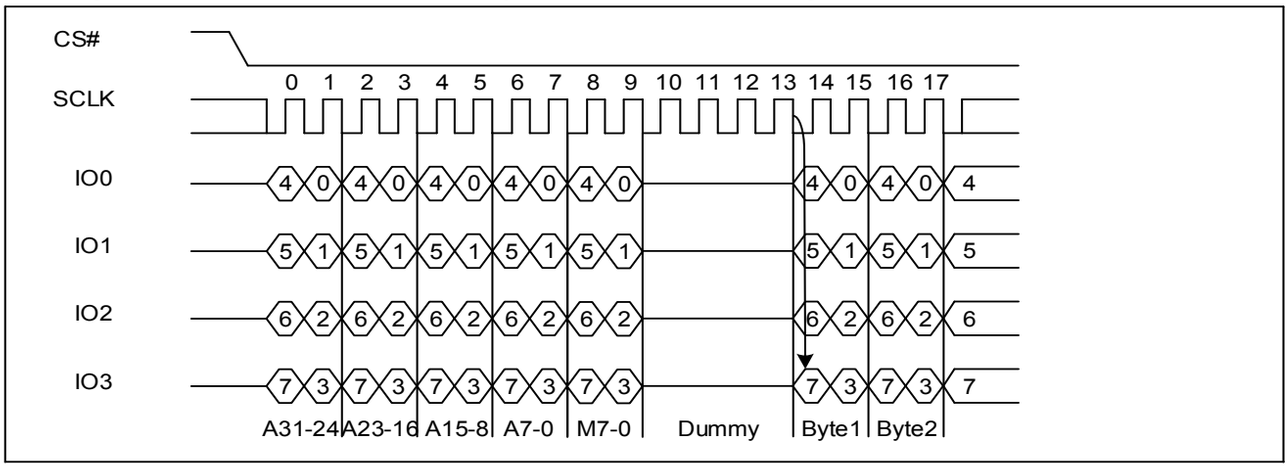


**Figure 33.Quad I/O Fast Read with 4-Byte Address Sequence Diagram (M5-4= (1, 0), ADS=0 or ADS=1)**




## Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH or ECH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH or ECH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-Byte section of a 256-Byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-Byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-Byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

## 8.14. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" command to access a fixed length of 8/16/32/64-Byte section within a 256-Byte page, in standard SPI mode.

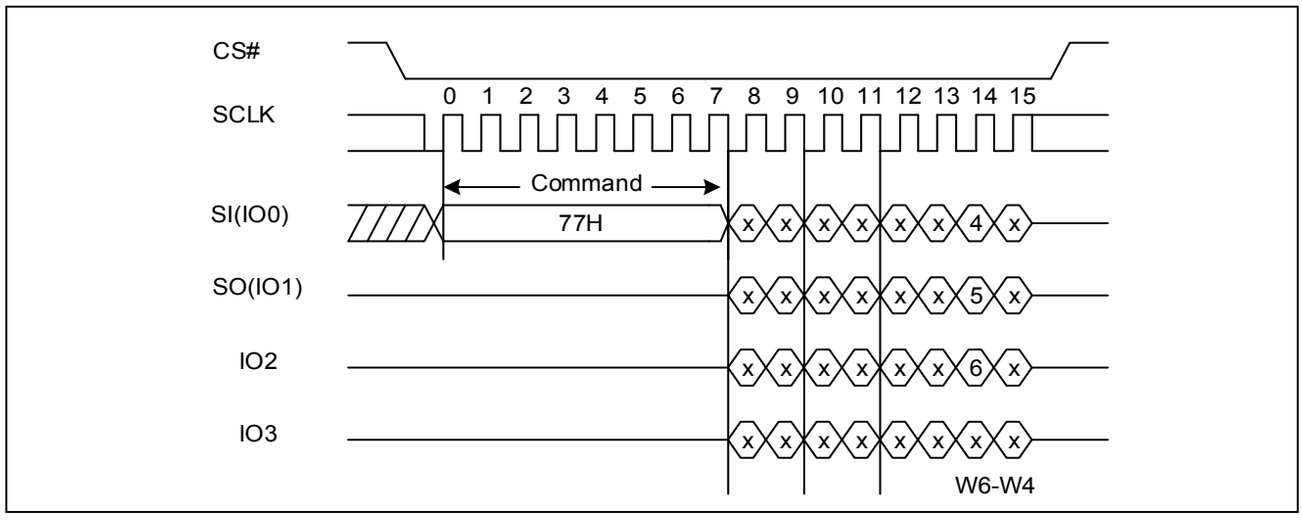
The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

**Table 15 Set Burst with Wrap configuration**

| W6,W5 | W4=0 | | W4=1 (default) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0, 0 | Yes | 8-Byte | No | N/A |
| 0, 1 | Yes | 16-Byte | No | N/A |
| 1, 0 | Yes | 32-Byte | No | N/A |
| 1, 1 | Yes | 64-Byte | No | N/A |

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-Byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

**Figure 34. Set Burst with Wrap Sequence Diagram**



## 8.15. Quad I/O DTR Read (EEH or EDH)

The DTRQIO instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the DTRQIO instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single DTRQIO instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DTRQIO instruction, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

While Program/Erase/Write Status Register cycle is in progress, DTRQIO instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

### Quad I/O DTR Read with "Continuous Read Mode"

The Quad I/O DTR Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input address. If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O DTR Read command (after CS# is raised and then lowered) does not require the EDH/EEH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first EDH/EEH command code, thus returning to normal operation. The only way to quit the Quad I/O DTR Continuous Read Mode" is to set the "Continuous Read Mode" bits (M5-4) not equal to (1,0).

**Figure 35. DTR Quad I/O Fast Read Sequence Diagram (ADS=0)**

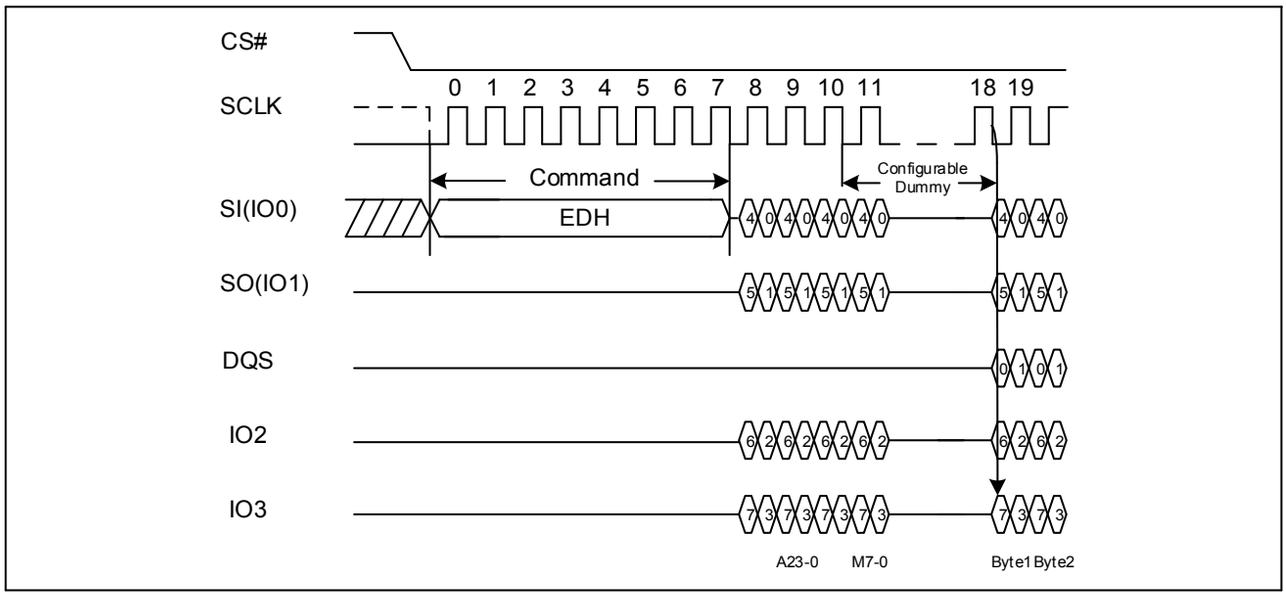


**Figure 36. DTR Quad I/O Fast Read Sequence Diagram (ADS=1)**

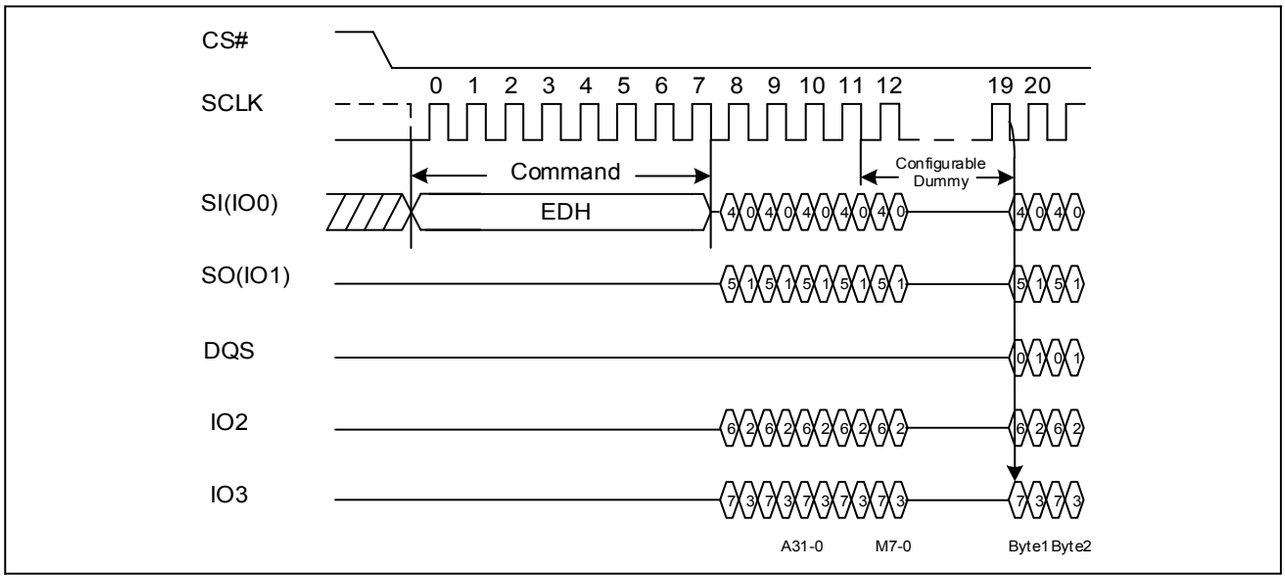



**Figure 37. DTR Quad I/O Fast Read Sequence Diagram (ADS=0 or ADS=1)**

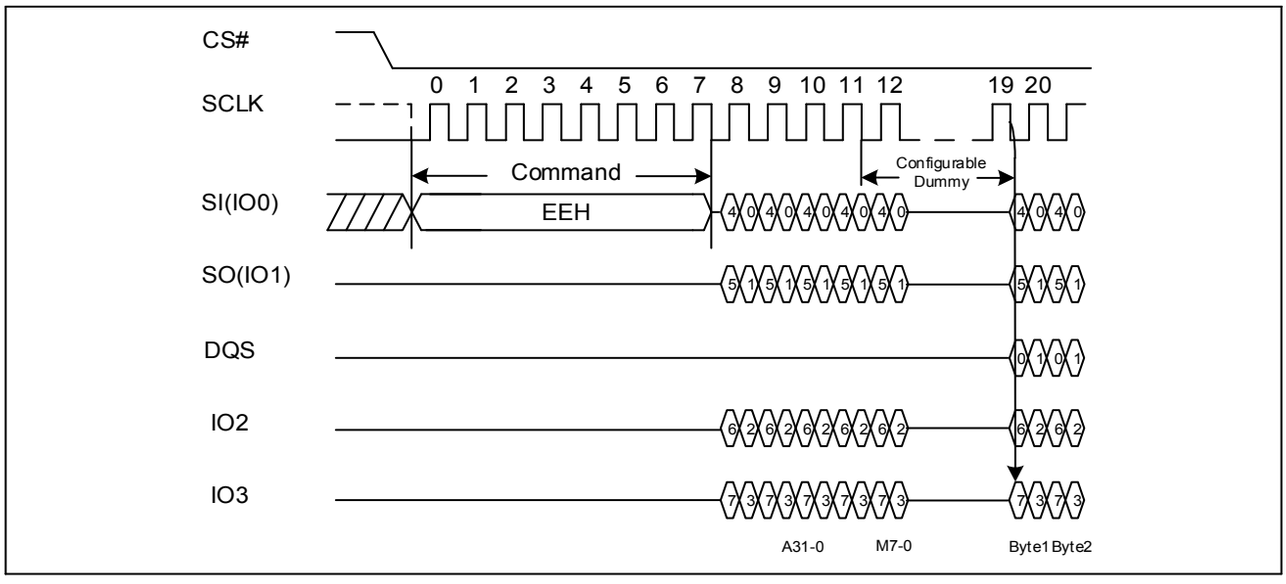


**Figure 38. DTR Quad I/O Fast Continuous Read Sequence Diagram (3-Byte Addr.)**

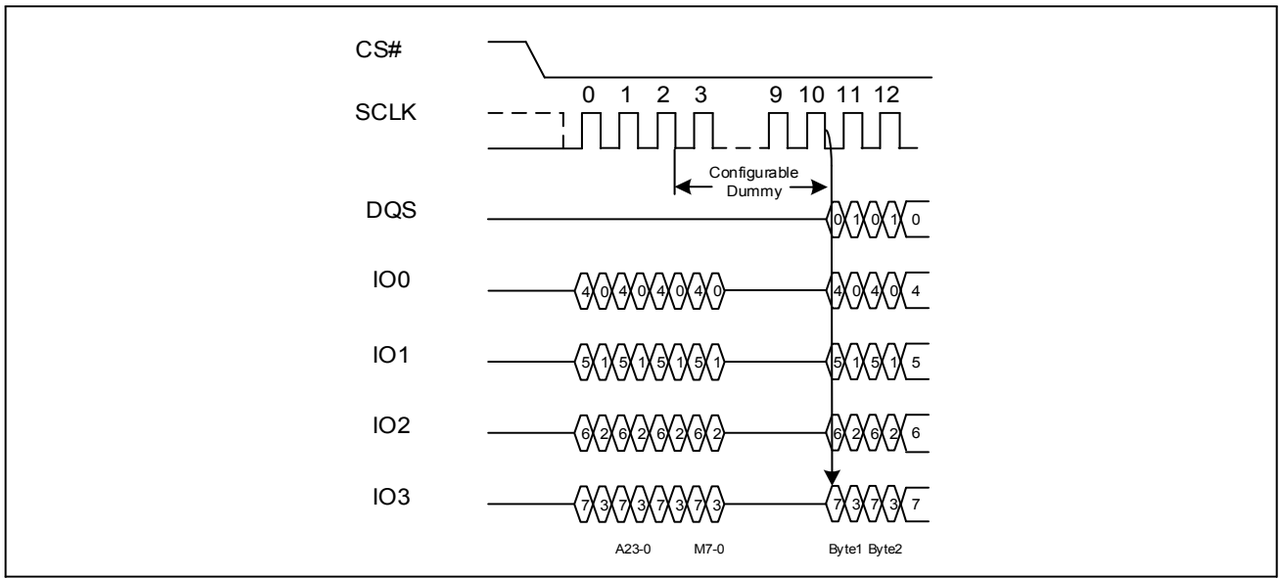
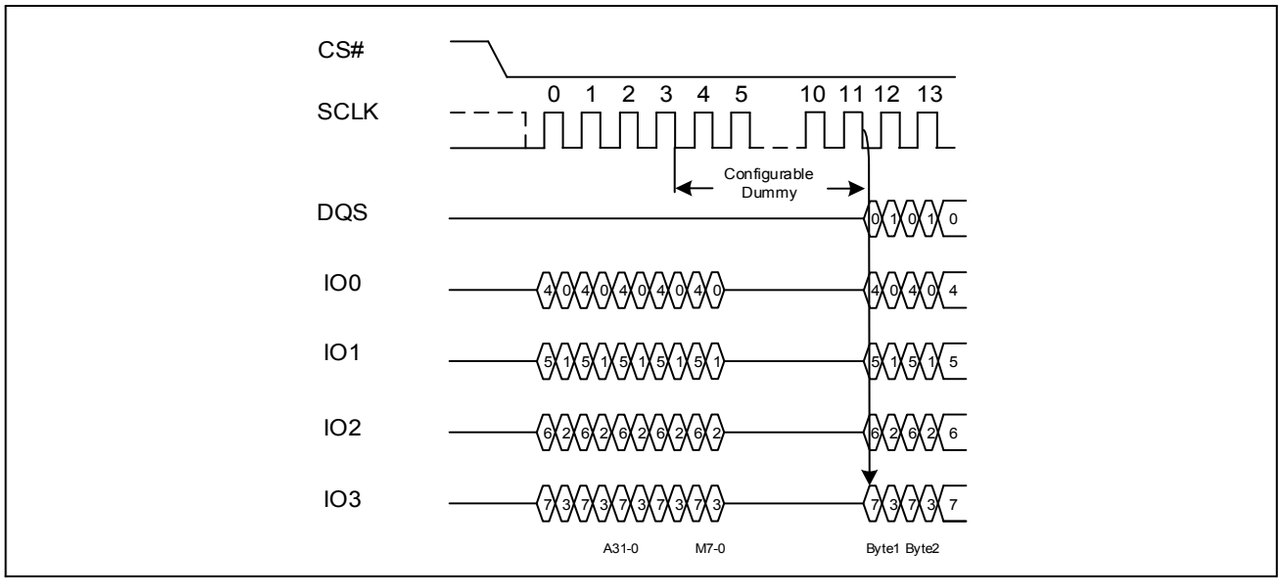


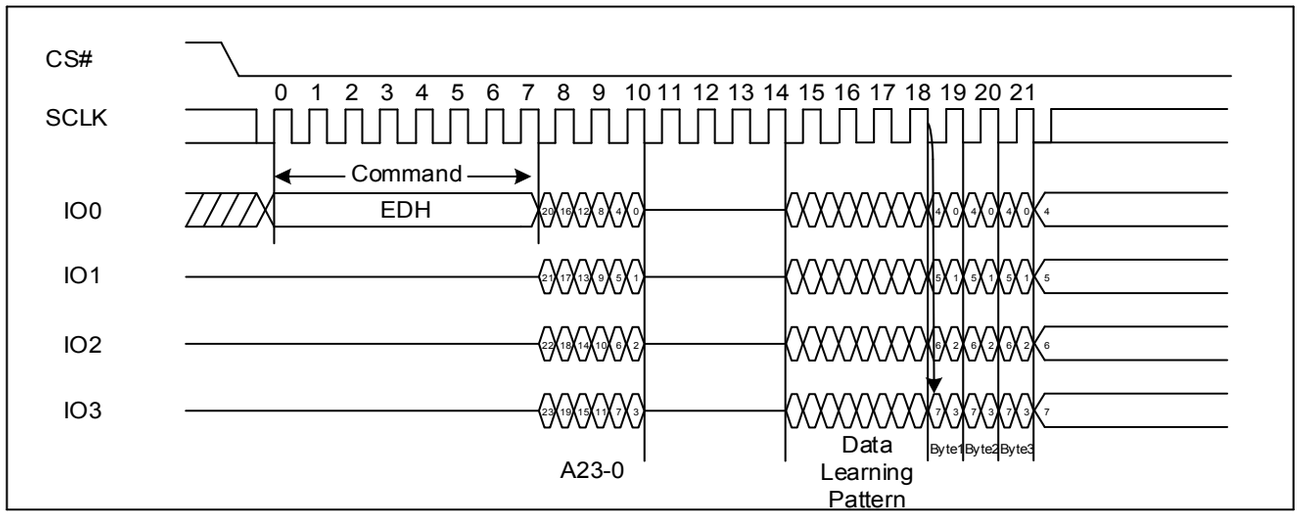

**Figure 39. DTR Quad I/O Fast Continuous Read Sequence Diagram (4-Byte Addr.)**



## 8.16. Write Data Learning Pattern (4AH)

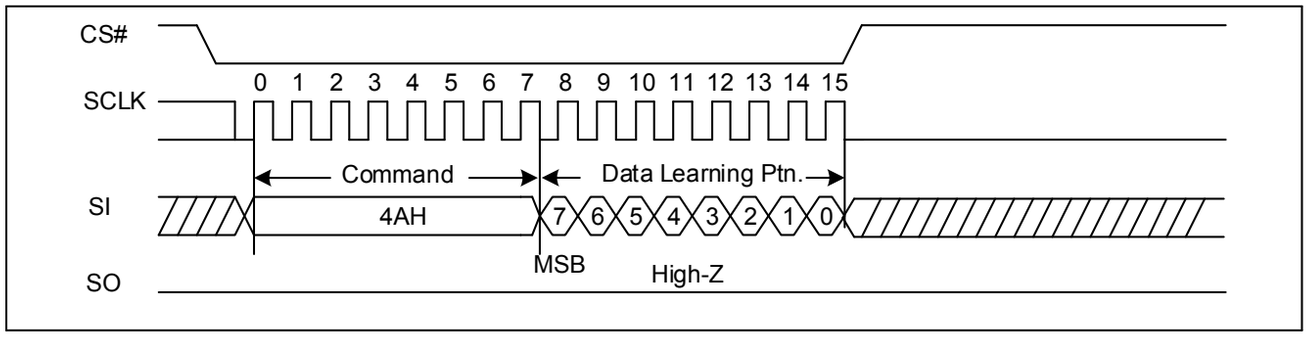
For Quad DTR Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, GD25B257D will output “00110100” Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output.

**Figure 40. Data Learning Pattern Output Sequence Diagram**




The Data Learning Pattern can also be defined by a “Write Data Learning Pattern (4AH)” command followed by 8-bit user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to its “00110100” default value.

**Figure 41. Write Data Learning Pattern Sequence Diagram**



## 8.17. Page Program (PP 02H or 4PP 12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address Bytes and at least one data Byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3 or 4-Byte address on SI → at least 1 Byte data on SI → CS# goes high. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is $t_{PP}$) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

When ECC is enabled (ECC=1 in Extended Register), Page Program instruction must program minimum aligned 8-Byte (A[2:0]=0,0,0) data or multiple of aligned 8-Byte data granularities, up to the 256-Byte page. Every aligned 8-Byte memory can only be programmed once before any Erase operation at that address.

**Figure 42. Page Program Sequence Diagram (ADS=0)**

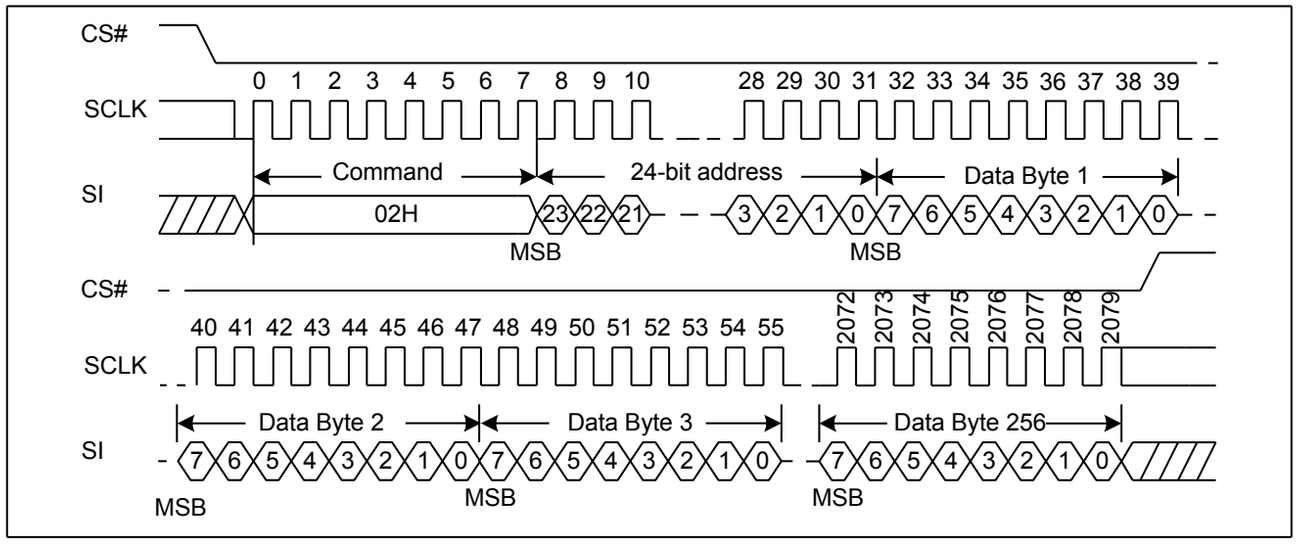


**Figure 43. Page Program Sequence Diagram (ADS=1)**

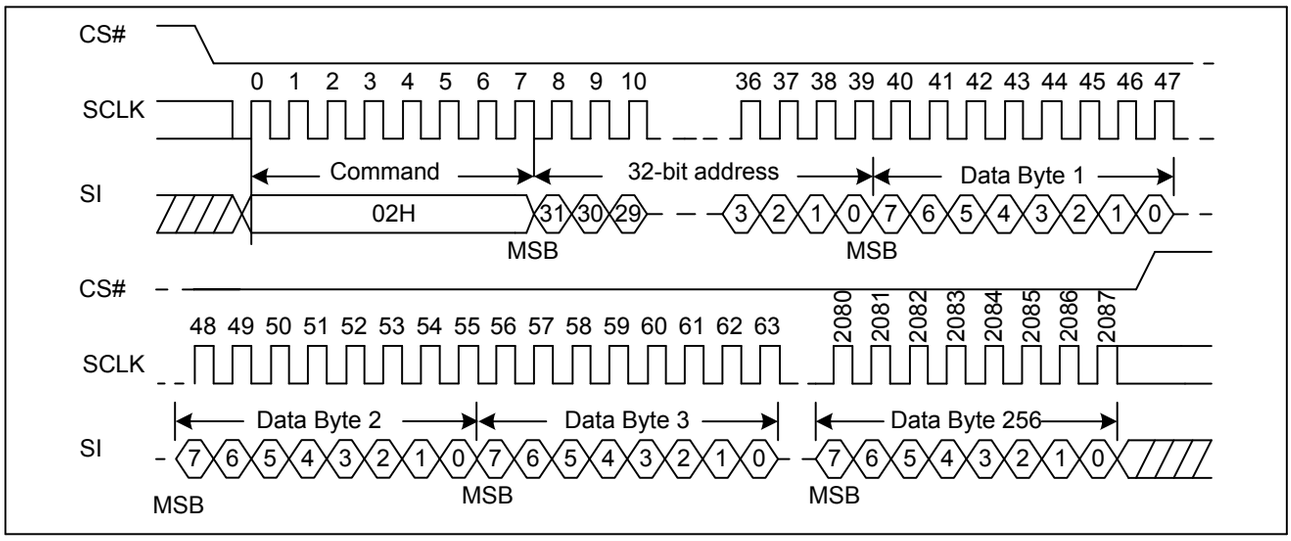
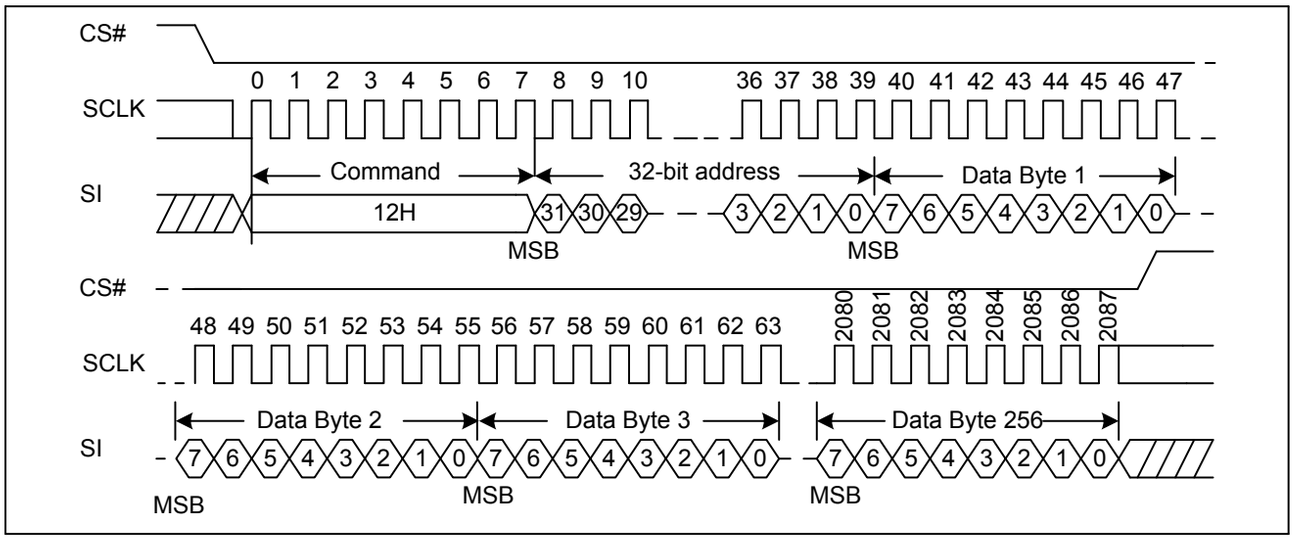



**Figure 44. Page Program with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.18. Quad Page Program (QPP 32H or 4QPP 34H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address Bytes and at least one data Byte on IO pins.

The command sequence is shown below. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. CS# must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is $t_{PP}$) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) is not executed.

When ECC is enabled (ECC=1 in Extended Register), Page Program instruction must program minimum aligned 8-Byte (A[2:0]=0,0,0) data or multiple of aligned 8-Byte data granularities, up to the 256-Byte page. Every aligned 8-Byte memory can only be programmed once before any Erase operation at that address.

**Figure 45. Quad Page Program Sequence Diagram (ADS=0)**

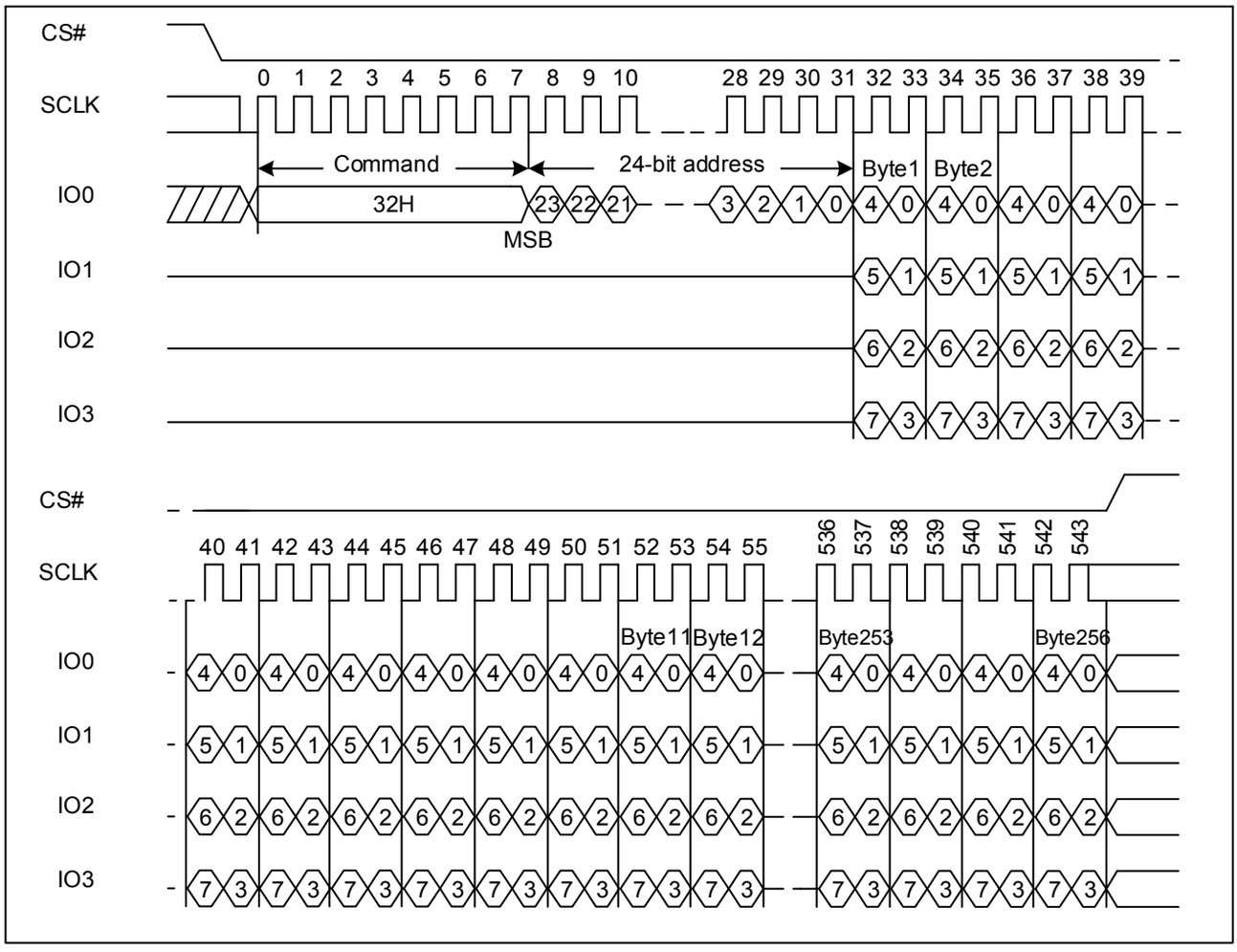


**Figure 46. Quad Page Program Sequence Diagram (ADS=1)**

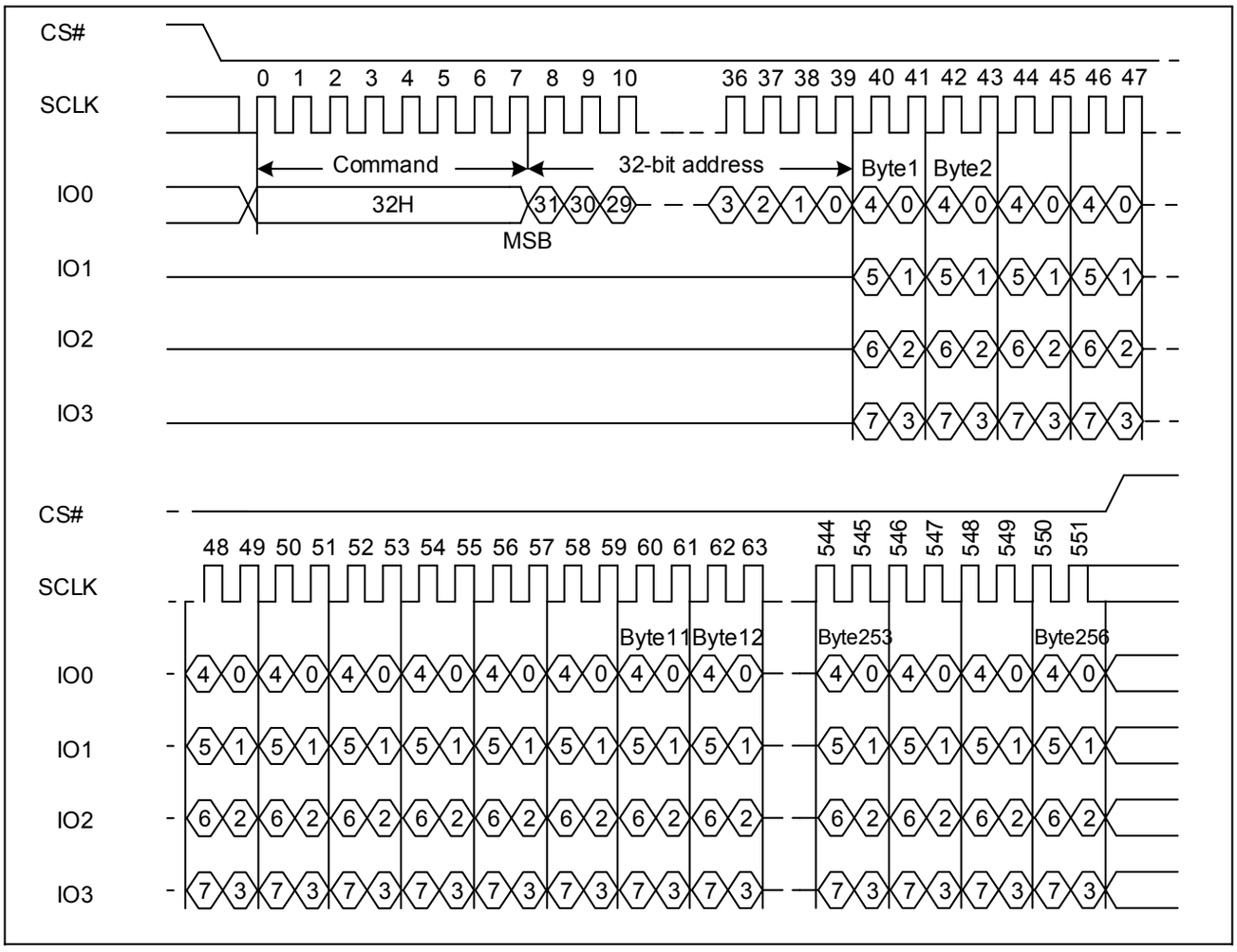
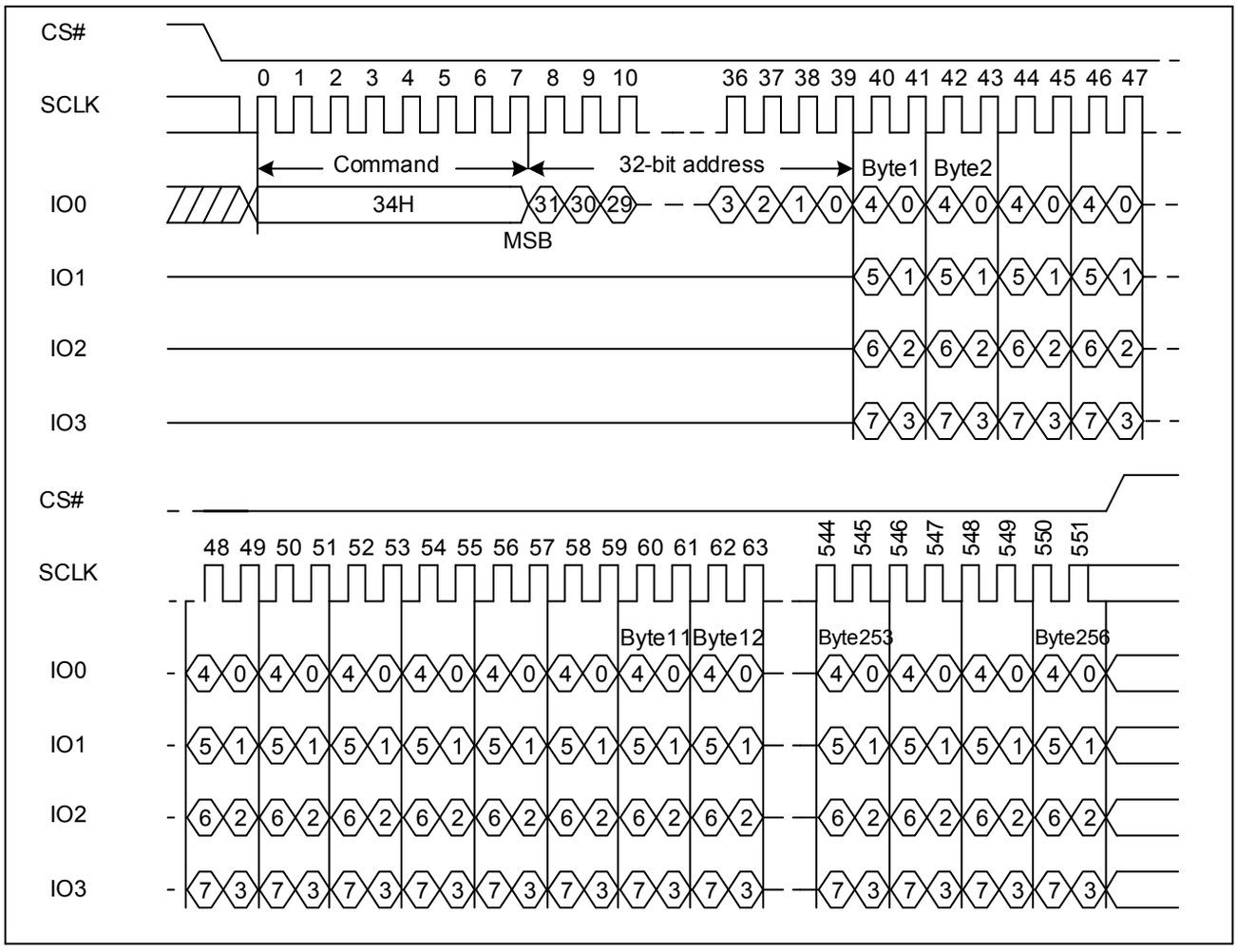


**Figure 47. Quad Page Program with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.19. Sector Erase (SE 20H or 4SE 21H)

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address Byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is $t_{SE}$) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bit is not executed.

**Figure 48. Sector Erase Sequence Diagram (ADS=0)**

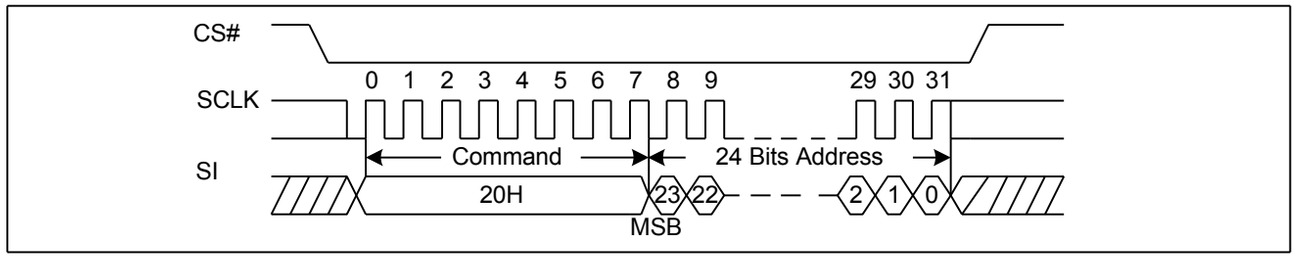



**Figure 49. Sector Erase Sequence Diagram (ADS=1)**

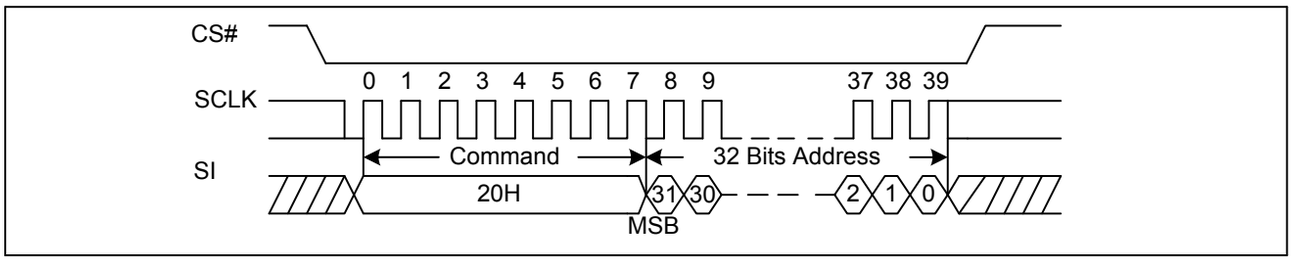
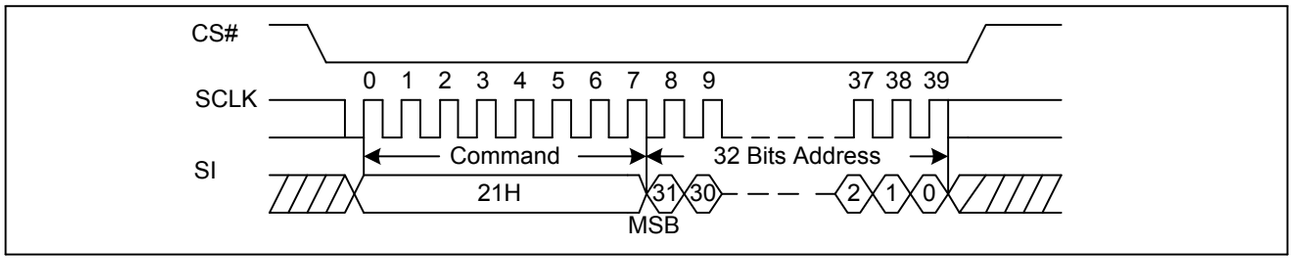



**Figure 50. Sector Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.20. 32KB Block Erase (BE32 52H or 4BE32 5CH)

The 32KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address Bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is $t_{BE}$) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits is not executed.

**Figure 51. 32KB Block Erase Sequence Diagram (ADS=0)**

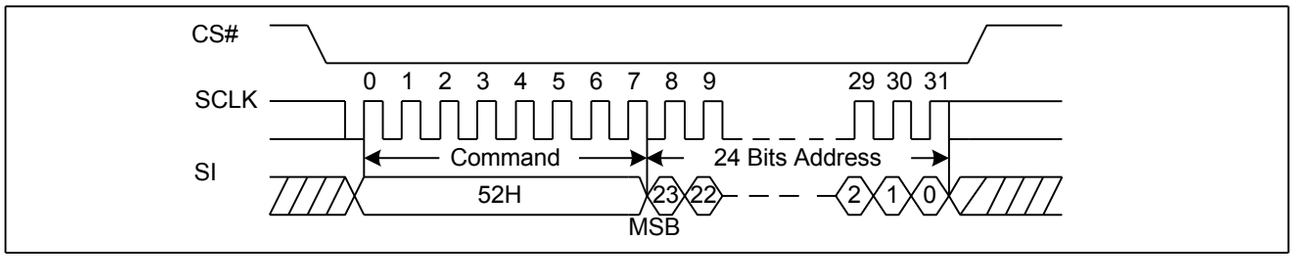



**Figure 52.32KB Block Erase Sequence Diagram (ADS=1)**

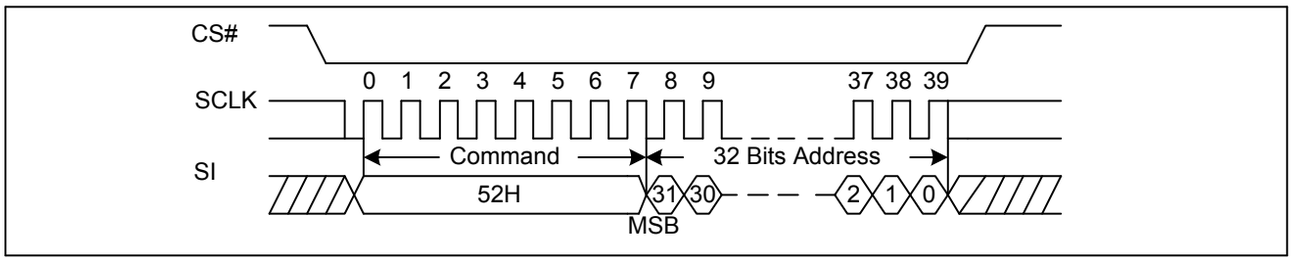
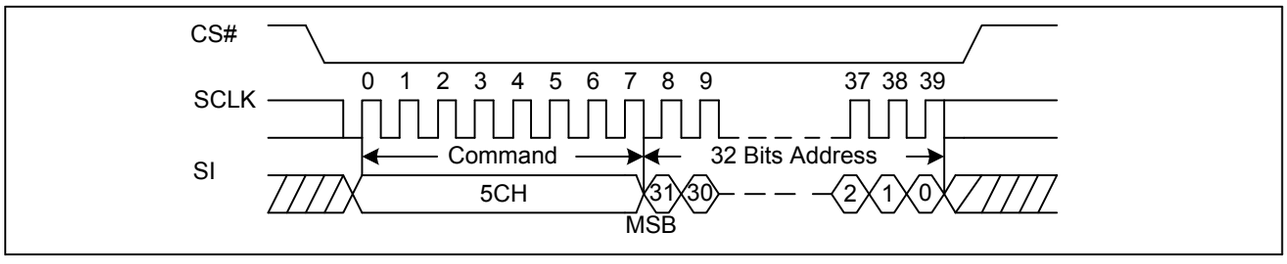



**Figure 53. 32KB Block Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**



## 8.21. 64KB Block Erase (BE64 D8H or 4BE64 DCH)

The 64KB Block Erase (BE) command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address Bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-Byte address on SI → CS# goes high. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is $t_{BE}$) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits is not executed.

**Figure 54. 64KB Block Erase Sequence Diagram (ADS=0)**

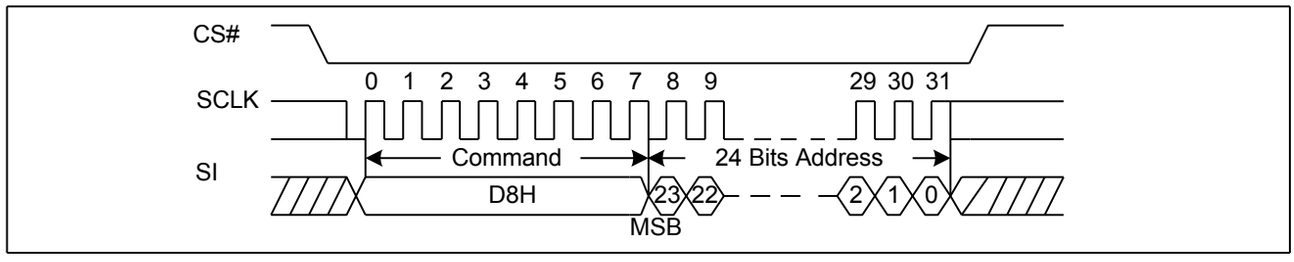



**Figure 55.64KB Block Erase Sequence Diagram (ADS=1)**

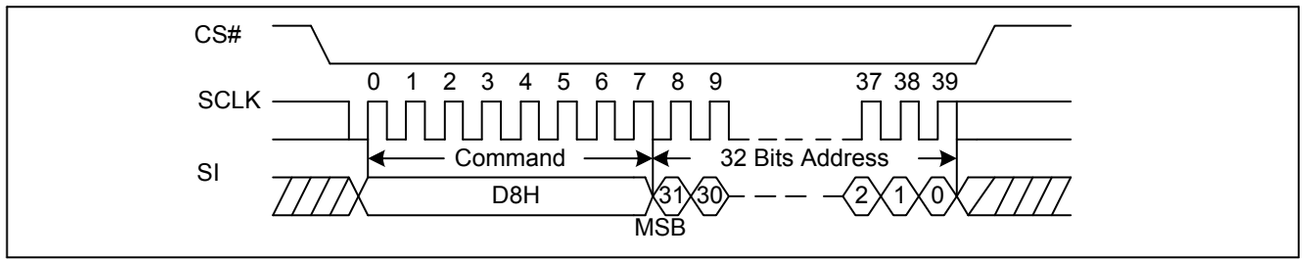
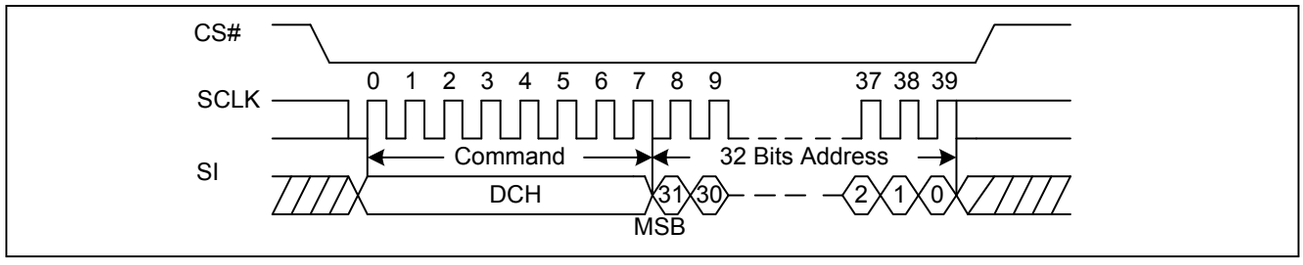



**Figure 56. 64KB Block Erase with 4-Byte Address Sequence Diagram (ADS=0 or ADS=1)**

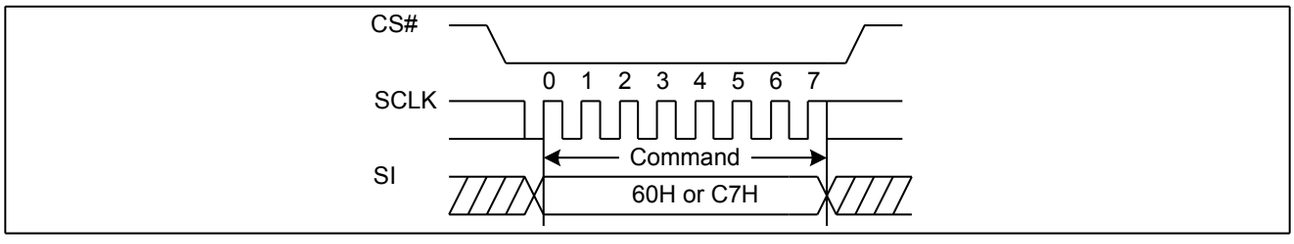


## 8.22. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is $t_{CE}$) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors/blocks are protected.

**Figure 57. Chip Erase Sequence Diagram**



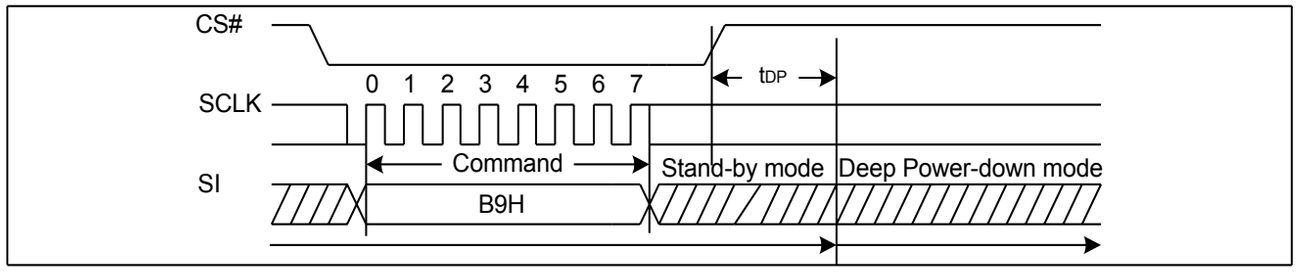
## 8.23. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command or software reset command. The Release from Deep Power-Down and Read Device ID (RDI) command releases the device from Deep Power-Down mode , also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always in the Standby Mode after Power-Up.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of $t_{DP}$ before the supply current is reduced to $I_{CC2}$ and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

**Figure 58. Deep Power-Down Sequence Diagram**



## 8.24. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence in 3 Byte mode (ADS=0): CS# goes low → sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 →Dummy Byte4→128bit Unique ID Out →CS# goes high.

The Read Unique ID command sequence in 4 Byte mode (ADS=1): CS# goes low → sending Read Unique ID command →Dummy Byte1 →Dummy Byte2 →Dummy Byte3 →Dummy Byte4→ Dummy Byte5→128bit Unique ID Out →CS# goes high.

**Figure 59. Read Unique ID Sequence Diagram (ADS=0)**

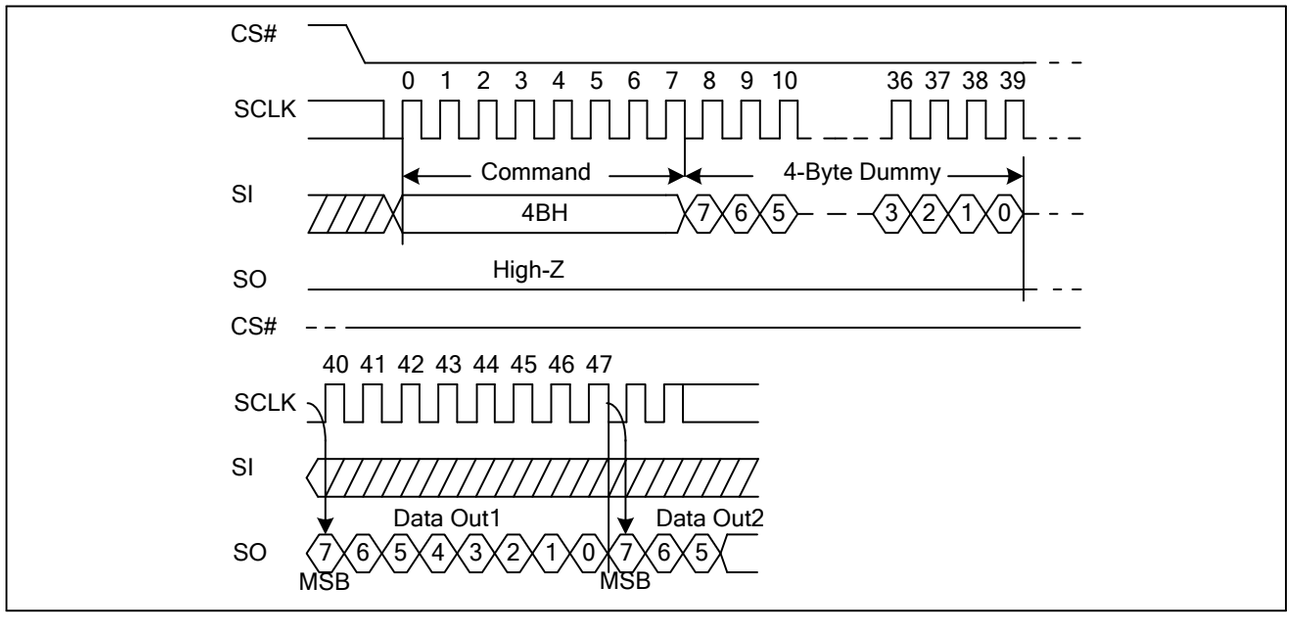
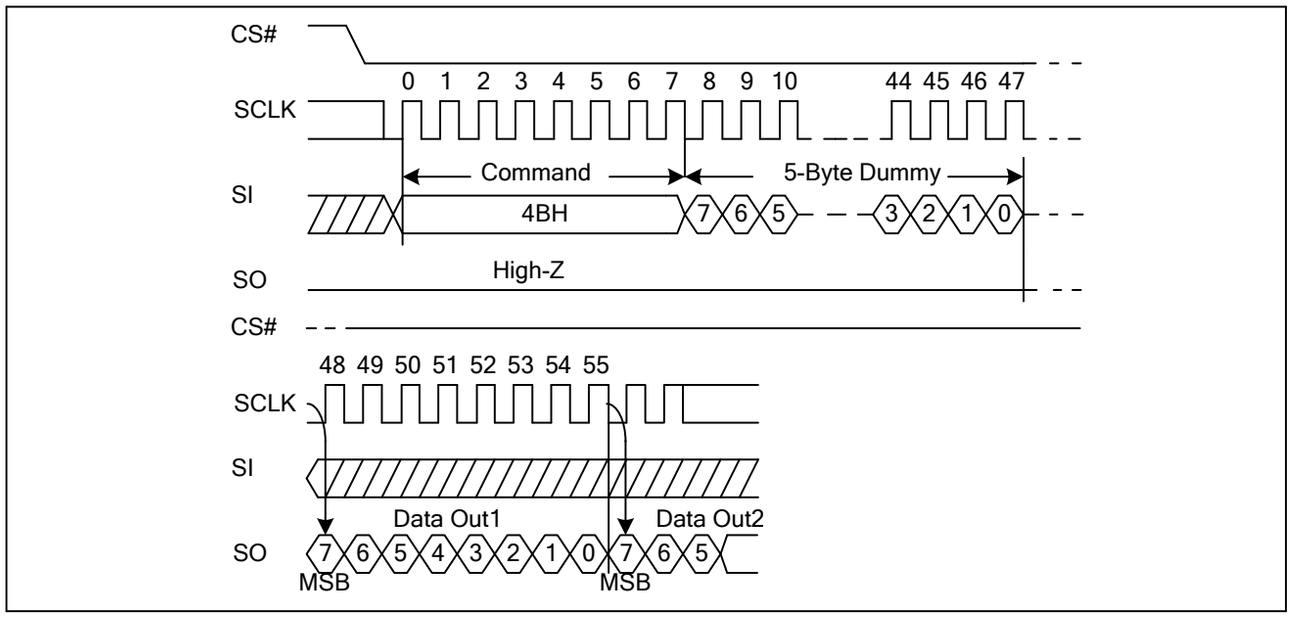



**Figure 60. Read Unique ID Sequence Diagram (ADS=1)**



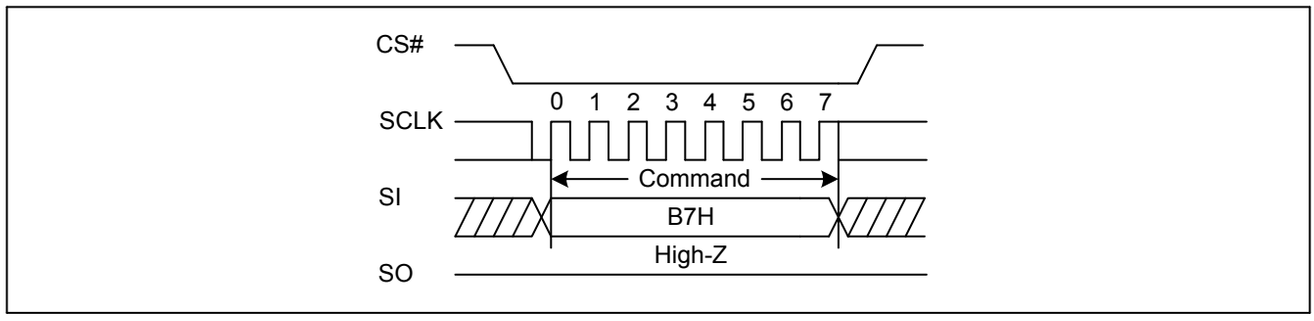
## 8.25. Enter 4-Byte Address Mode (B7H)

The Enter 4-Byte Address Mode command enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit8 (ADS bit) of status register will be automatically set to "1" to indicate the 4-Byte address mode has been enabled. Once the 4-Byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Enter 4-Byte mode command →CS# goes high.

**Figure 61. Enter 4-Byte Address Mode Sequence Diagram**

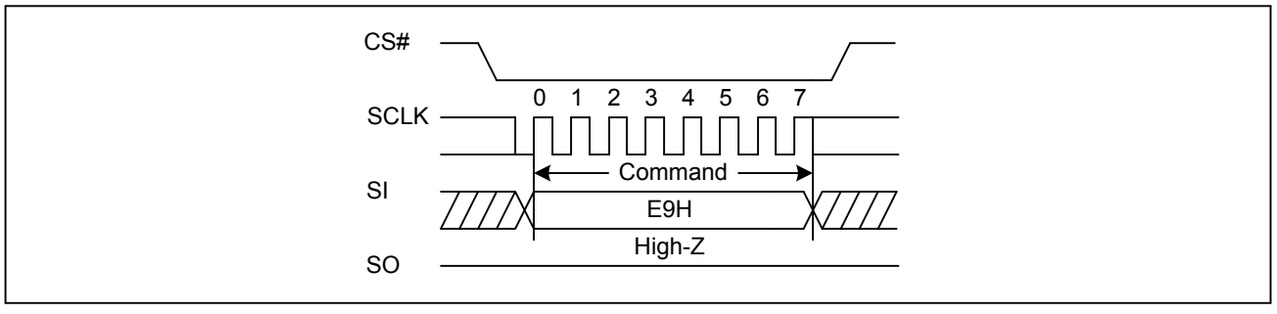



## 8.26. Exit 4-Byte Address Mode (E9H)

The Exit 4-Byte Address Mode command is executed to exit the 4-Byte address mode and return to the default 3-Byte address mode. After sending out the EX4B instruction, the bit8 (ADS bit) of status register will be cleared to "0" to indicate the exit of the 4-Byte address mode. Once exiting the 4-Byte address mode, the address length will return to 24-bit.

The sequence of issuing EN4B instruction is: CS# goes low → sending Exit 4-Byte Address Mode command →CS# goes high.

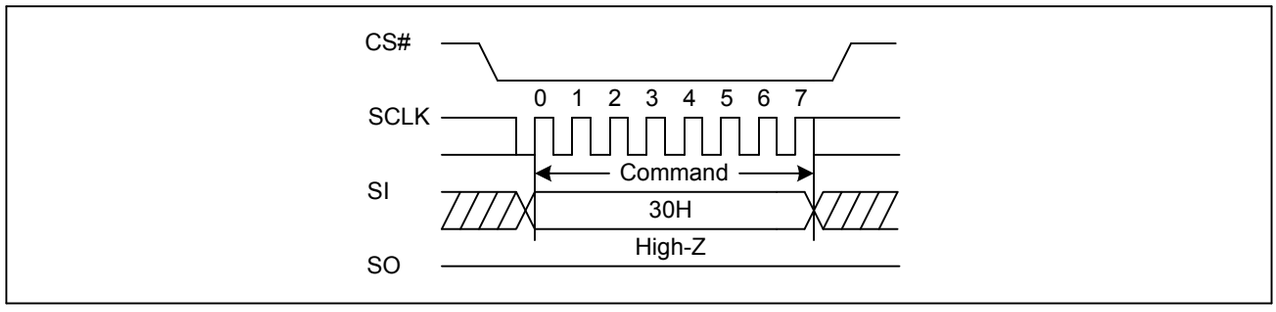
**Figure 62.Exit 4-Byte Address Mode Sequence Diagram**



## 8.27. Clear SR Flags (30H)

The Clear Status Register Flags command resets bit S18 (Program Error bit) and S19 (Erase Error bit) from status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will be not accepted even when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

**Figure 63.Clear Status Register Flags Sequence Diagram**




## 8.28. Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown below. Release from Power-Down will take the time duration of $t_{RES1}$ (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the $t_{RES1}$ time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy Byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, except that after CS# is driven high it must remain high for a time duration of $t_{RES2}$ (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

**Figure 64. Release Power-Down Sequence Diagram**

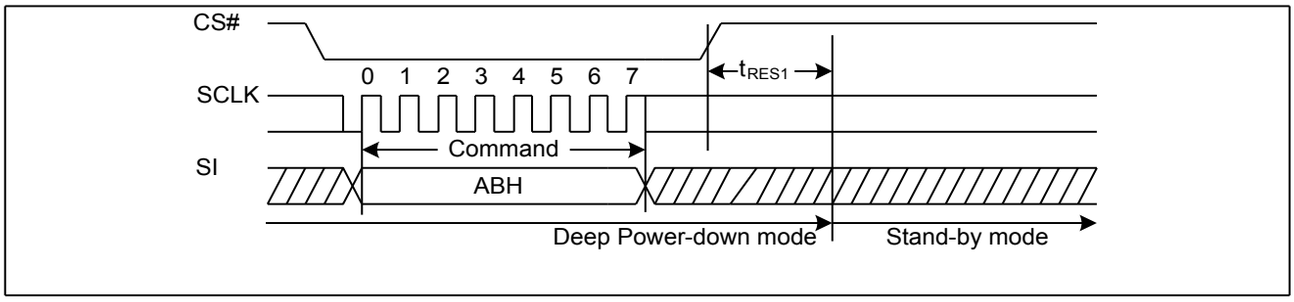
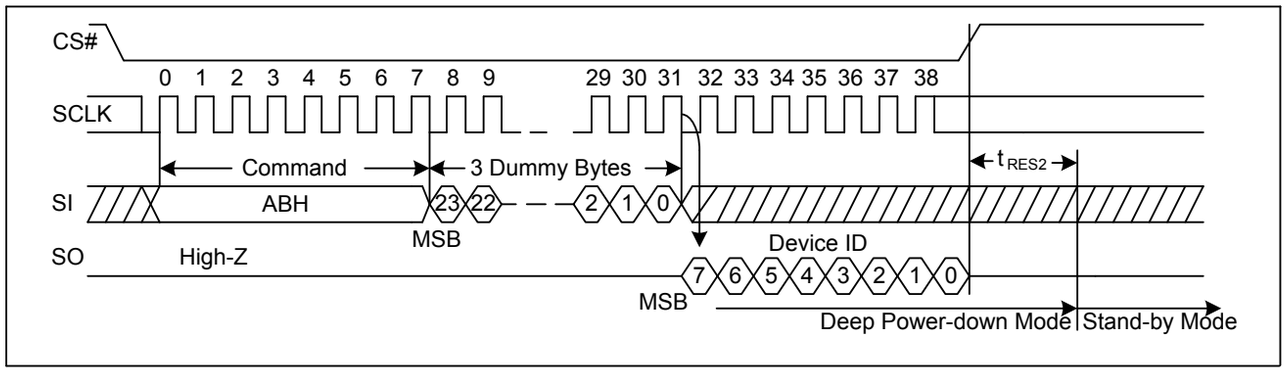


**Figure 65. Release Power-Down/Read Device ID Sequence Diagram**

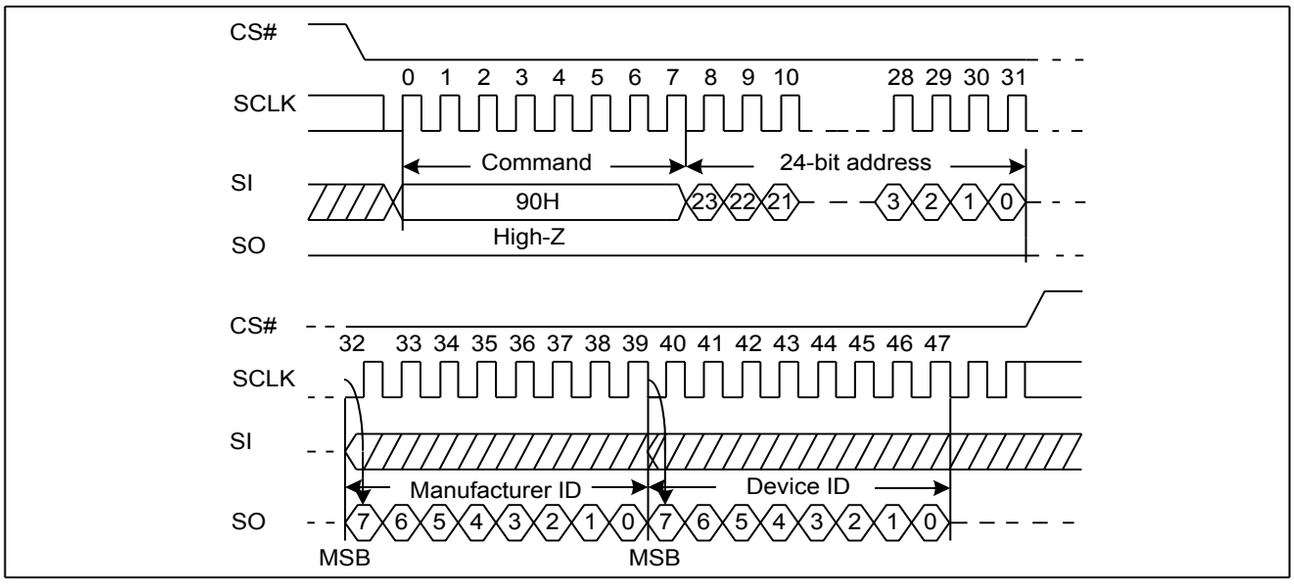



## 8.29. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

**Figure 66. Read Manufacture ID/ Device ID Sequence Diagram**

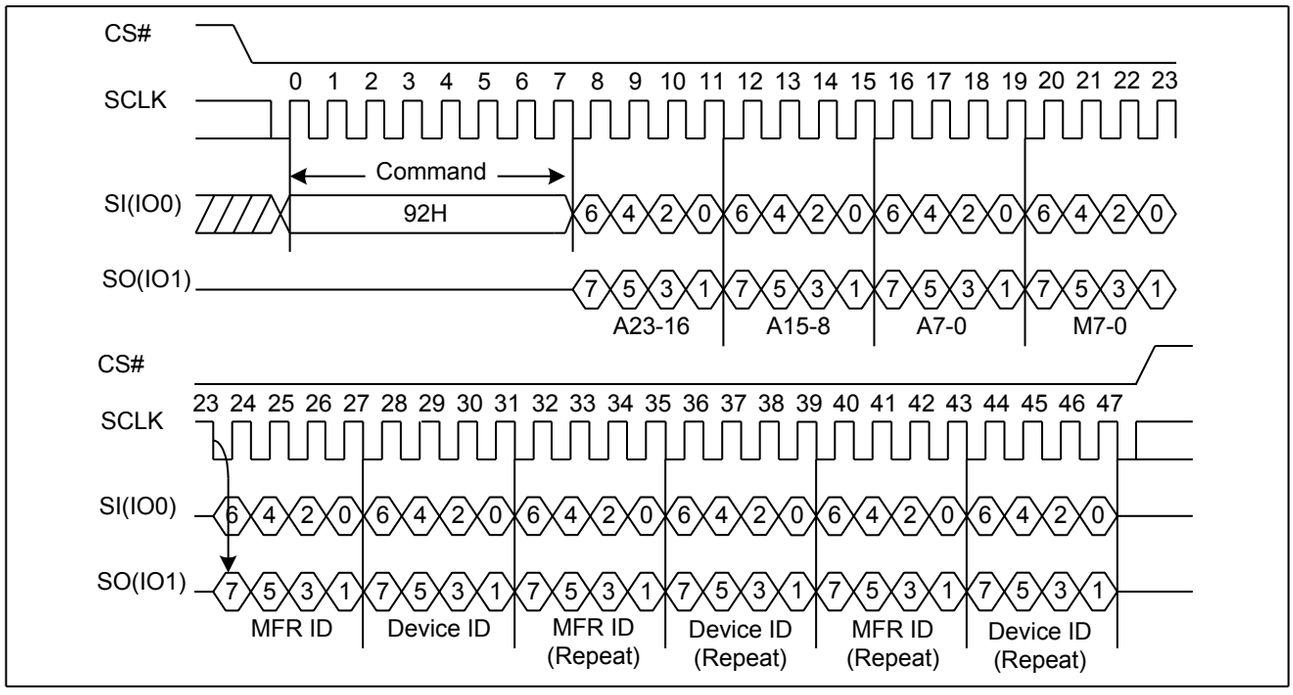


## 8.30. Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

**Figure 67. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram**

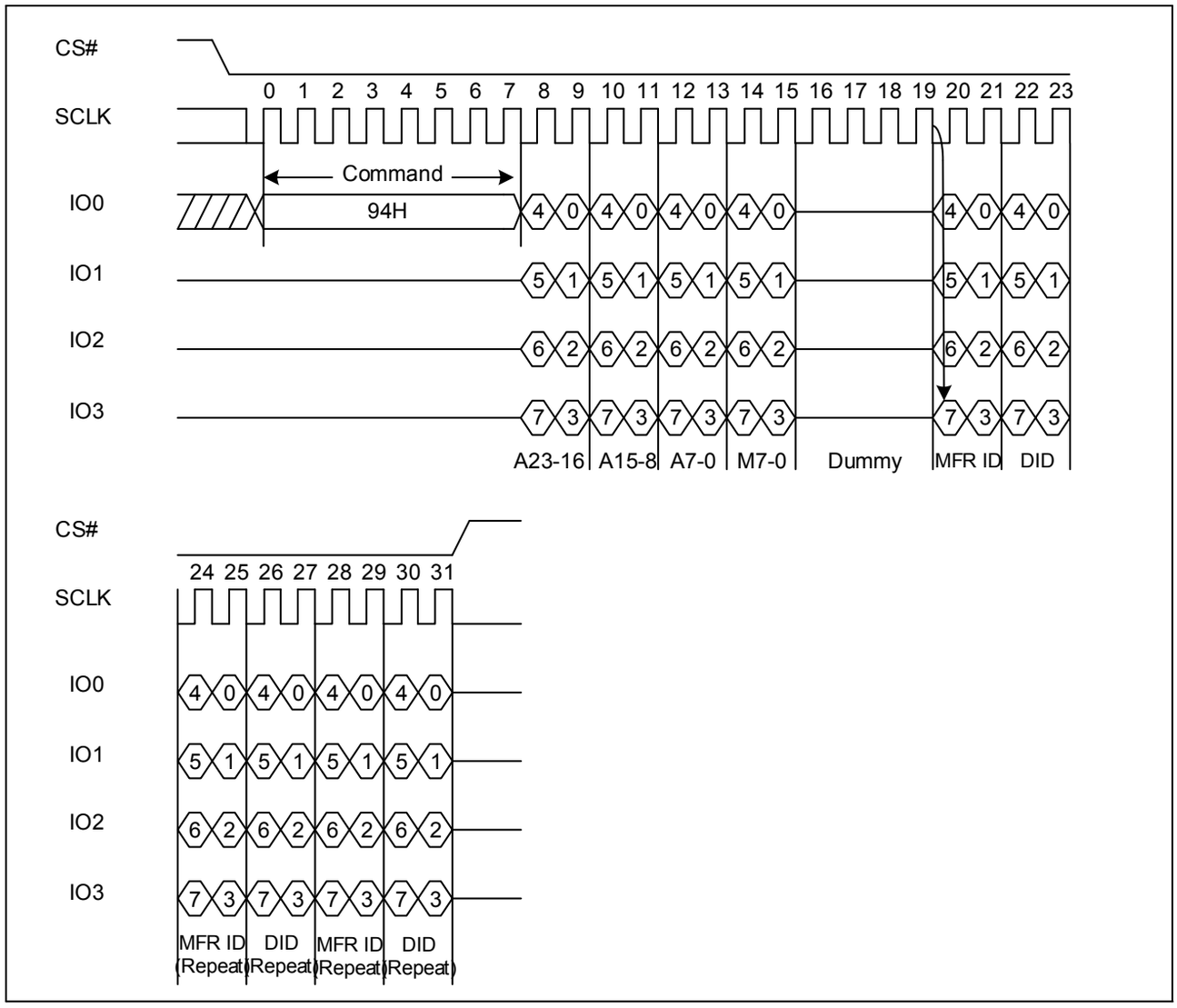


## 8.31. Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code “94H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

**Figure 68. Read Manufacture ID/ Device ID Quad I/O Sequence Diagram**

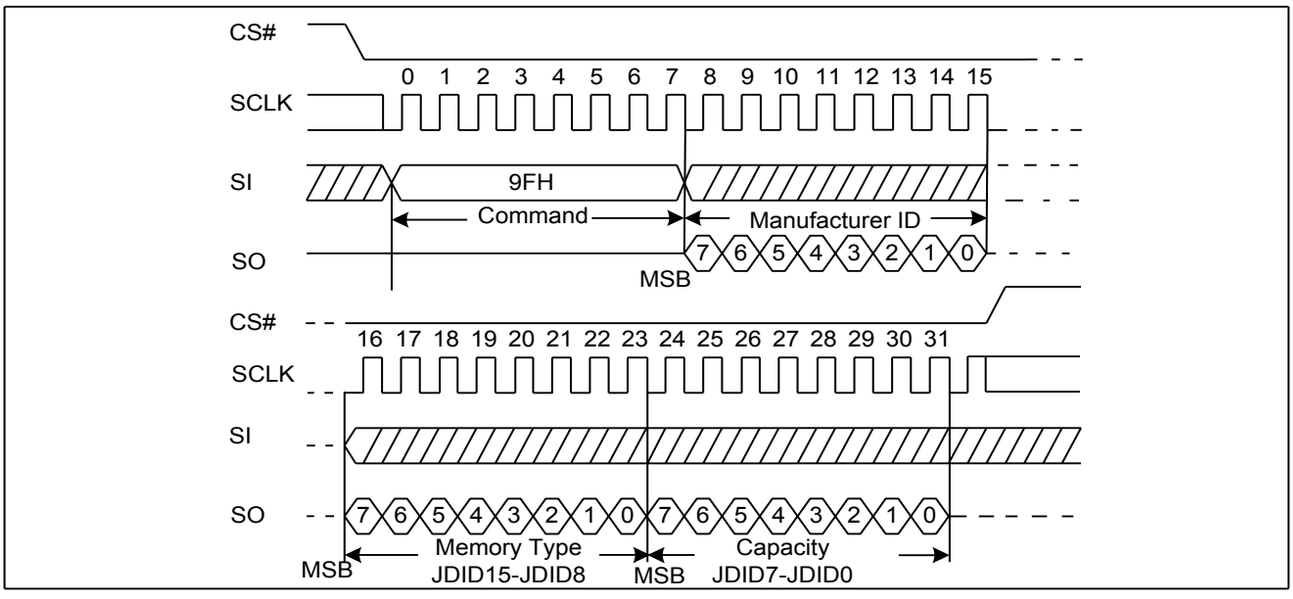


## 8.32. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two Bytes of device identification. The device identification indicates the memory type in the first Byte, and the memory capacity of the device in the second Byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory. Each bit is shifted out on the falling edge of Serial Clock. The Read Identification (RDID) command is terminated by driving CS# high at any time during data output. When CS# is driven high, the device is in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

**Figure 69. Read Identification ID Sequence Diagram**



## 8.33. Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Status Register command (01H, 31H, 11H) and Erase/Program Security Registers command (44H, 42H), Erase commands(20H, 21H, 52H, 5CH, D8H, DCH, C7H, 60H) and Page Program command (02H, 12H, 32H, 34H) are not allowed during Program suspend. The Write Status Register command (01H, 31H, 11H), Erase Security Registers command (44H) and Erase commands (20H, 21H, 52H, 5CH, D8H, DCH, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation.

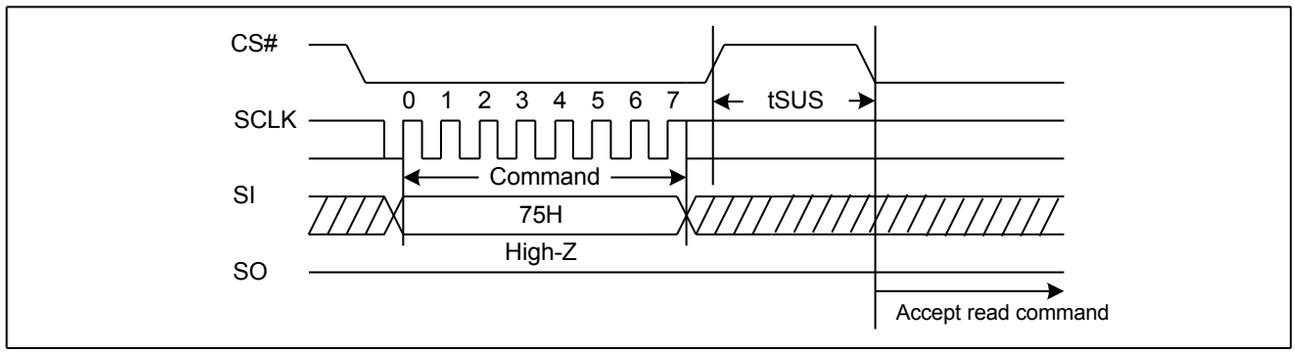
**Table 16. Commands Allowed During Program or Erase Suspend**

| Command Name | Code (Hex) | Allowed During Erase Suspend | Allowed During Program Suspend | Comment |
|---|---|---|---|---|
| Write Enable | 06 | Yes | | Required for program command within erase suspend. |
| Read Status Register-1 | 05 | Yes | Yes | Needed to read WIP to determine end of suspend process. |
| Read Status Register-2 | 35 | Yes | Yes | Needed to read suspend status to determine whether the operation is suspended or complete. |
| Read Status Register-3 | 15 | Yes | Yes | Needed to read suspend status to determine whether the operation is suspended or complete. |
| Read Extended Addr. Register | C8 | Yes | Yes | Extended Addr. Register may need to be changed during a suspend to reach a sector needed for read or program. |
| Write Extended Addr. Register | C5 | Yes | Yes | Extended Addr. Register may need to be changed during a suspend to reach a sector needed for read or program. |
| Read | 03 | Yes | Yes | All array reads allowed in suspend. |
| 4Read | 13 | Yes | Yes | All array reads allowed in suspend. |
| Fast Read | 0B | Yes | Yes | All array reads allowed in suspend. |
| 4Fast Read | 0C | Yes | Yes | All array reads allowed in suspend. |
| Dual I/O Fast Read | BB | Yes | Yes | All array reads allowed in suspend. |
| 4Dual I/O Fast Read | BC | Yes | Yes | All array reads allowed in suspend. |
| Dual Output Fast Read | 3B | Yes | Yes | All array reads allowed in suspend. |
| 4Dual Output Fast Read | 3C | Yes | Yes | All array reads allowed in suspend. |
| Quad I/O Fast Read | EB | Yes | Yes | All array reads allowed in suspend. |
| 4Quad I/O Fast Read | EC | Yes | Yes | All array reads allowed in suspend. |
| Quad Output Fast Read | 6B | Yes | Yes | All array reads allowed in suspend. |
| 4Quad Output Fast Read | 6C | Yes | Yes | All array reads allowed in suspend. |
| Page Program | 02 | Yes | | Required for array program during erase suspend. |
| 4Page Program | 12 | Yes | | Required for array program during erase suspend. |

| | | | | |
|---|---|---|---|---|
| Quad Page Program | 32 | Yes | | Required for array program during erase suspend. |
| 4Quad Page Program | 34 | Yes | | Required for array program during erase suspend. |
| Program/Erase Resume | 7A | Yes | | Required to resume from erase/program suspend. |
| Enable Reset | 66 | Yes | Yes | Reset allowed anytime. |
| Reset | 99 | Yes | Yes | Reset allowed anytime. |

The Program/Erase Suspend command will be accepted by the device only if the SUS2/SUS1 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS2/SUS1 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS2/SUS1 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

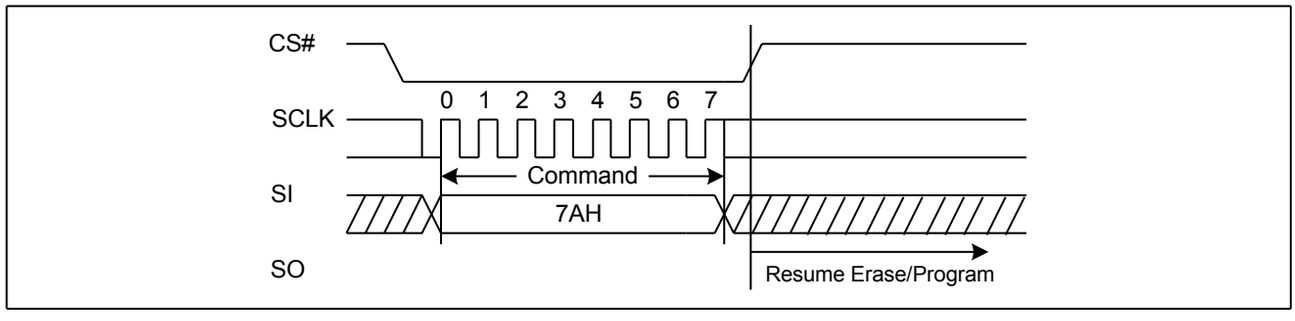
**Figure 70. Program/Erase Suspend Sequence Diagram**




## 8.34. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS2/SUS1 bit equal to 1 and the WIP bit equal to 0. After issued the SUS2/SUS1 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

**Figure 71. Program/Erase Resume Sequence Diagram**



## 8.35. Erase Security Registers (44H)

The GD25B257D provides three 2048-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command →3 or 4-Byte address on SI → CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is $t_{SE}$) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

**Table 17. Security Registers**

| Address | A23-16 | A15-12 | A11 | A10-0 |
|---|---|---|---|---|
| Security Register #1 | 00H | 0 0 0 1 | 0 | Don't care |
| Security Register #2 | 00H | 0 0 1 0 | 0 | Don't care |
| Security Register #3 | 00H | 0 0 1 1 | 0 | Don't care |

**Figure 72. Erase Security Registers command Sequence Diagram (ADS=0)**

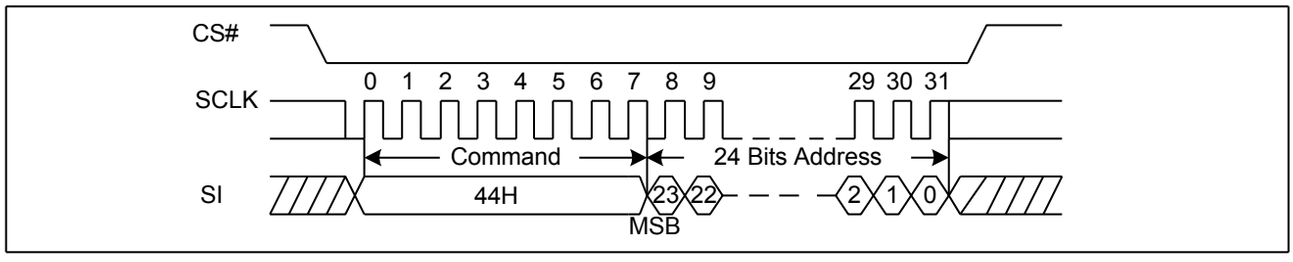
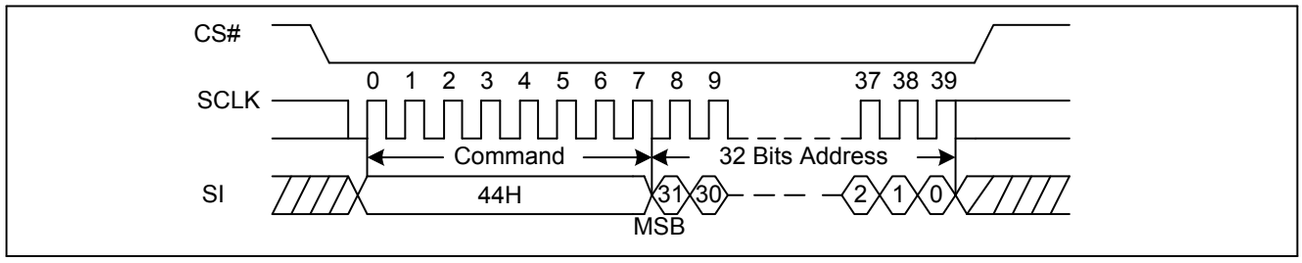



**Figure 73.Erase Security Registers command Sequence Diagram (ADS=1)**



## 8.36. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address Bytes and at least one data Byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is $t_{PP}$) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

**Table 18. Security Registers**

| Address | A23-16 | A15-12 | A11 | A10-0 |
|---|---|---|---|---|
| Security Register #1 | 00H | 0 0 0 1 | 0 | Byte Address |
| Security Register #2 | 00H | 0 0 1 0 | 0 | Byte Address |
| Security Register #3 | 00H | 0 0 1 1 | 0 | Byte Address |

**Figure 74. Program Security Registers command Sequence Diagram (ADS=0)**

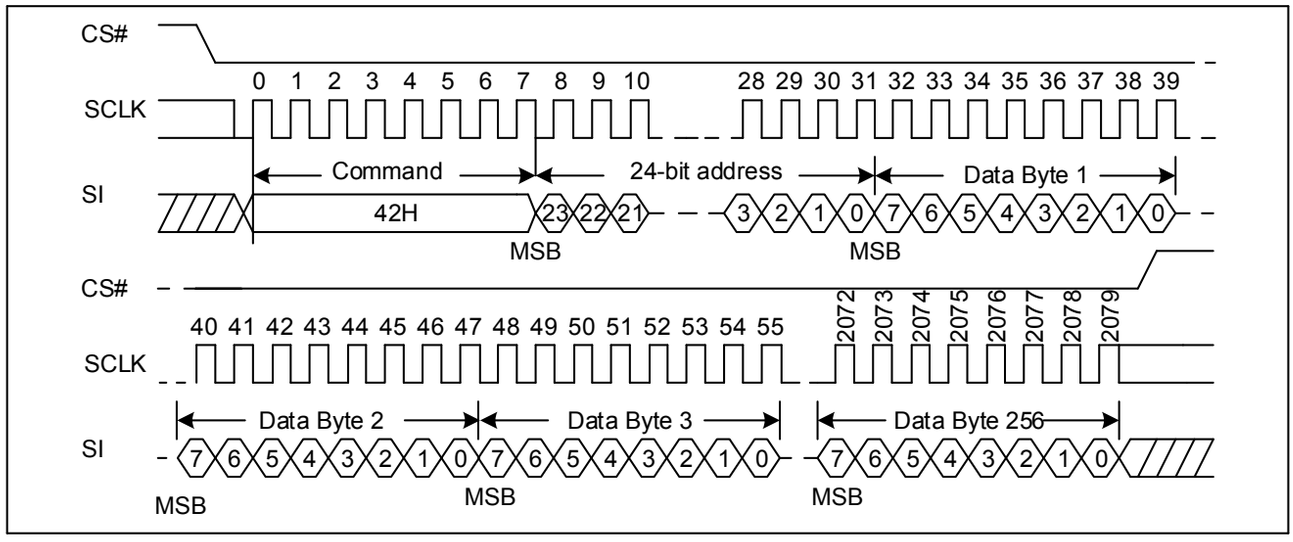
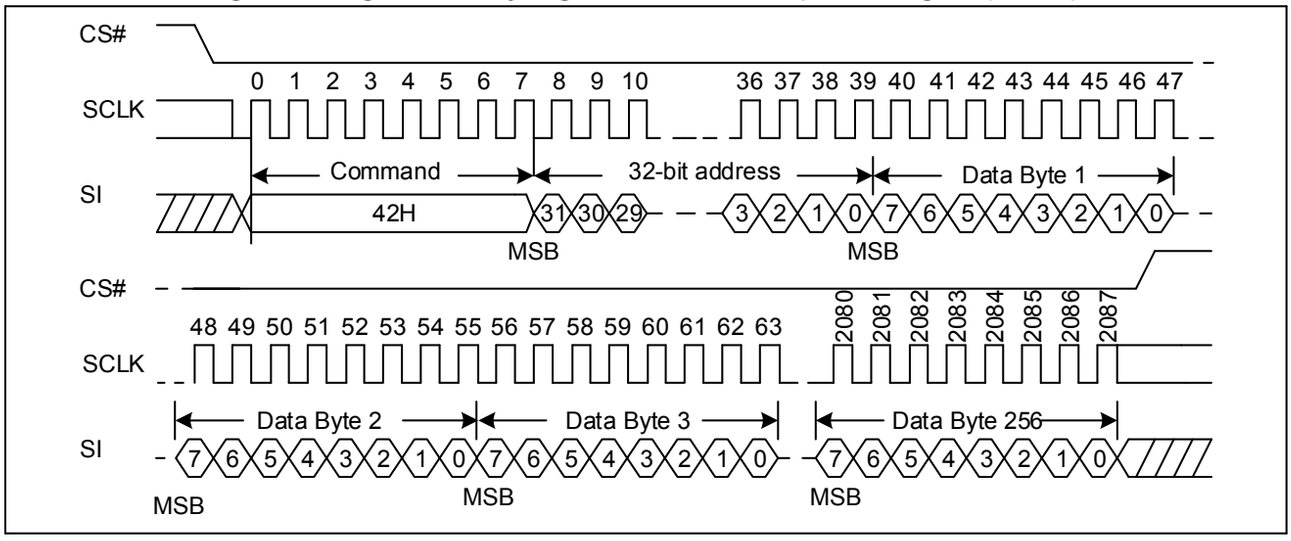



**Figure 75.Program Security Registers command Sequence Diagram (ADS=1)**



## 8.37. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command i is followed by a 3-Byte address (A23-A0) or 4-Byte address (A31-A0) and a dummy Byte, and each bit being latched-in on the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, and each bit being shifted out, at a Max frequency $f_C$, on the falling edge of SCLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. Once the A10-A0 address reaches the last Byte of the register (Byte 7FFH), it will reset to 000H, the command is completed by driving CS# high.

**Table 19. Security Registers**

| Address | A23-16 | A15-12 | A11 | A10-0 |
|---|---|---|---|---|
| Security Register #1 | 00H | 0 0 0 1 | 0 | Byte Address |
| Security Register #2 | 00H | 0 0 1 0 | 0 | Byte Address |
| Security Register #3 | 00H | 0 0 1 1 | 0 | Byte Address |

**Figure 76. Read Security Registers command Sequence Diagram (ADS=0)**

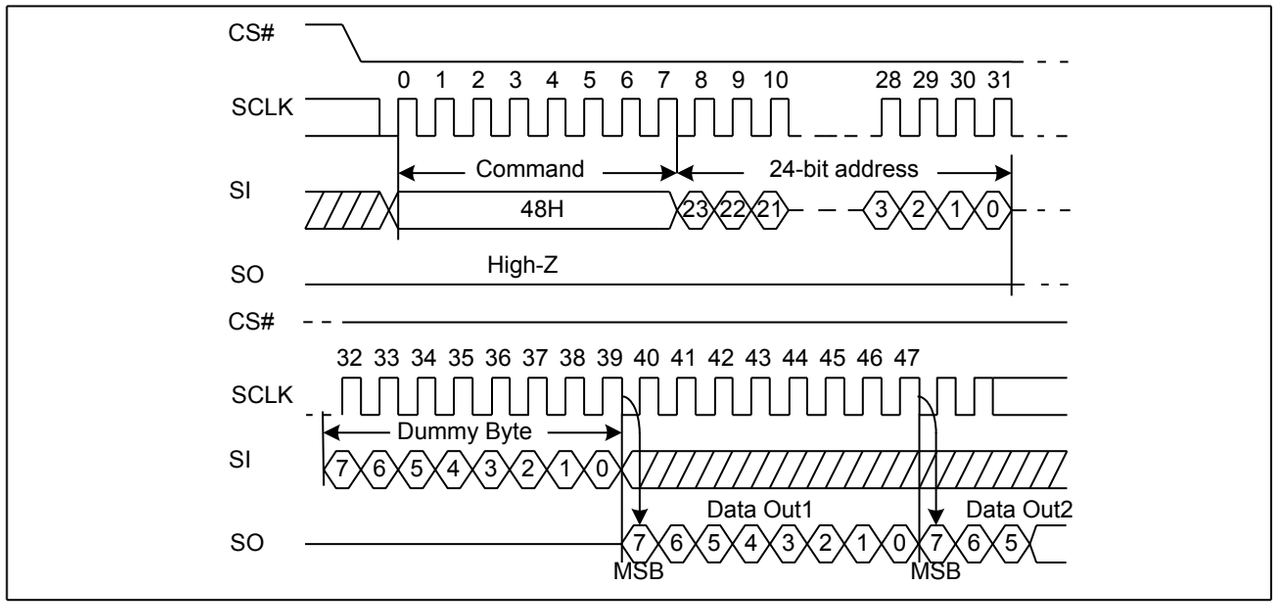
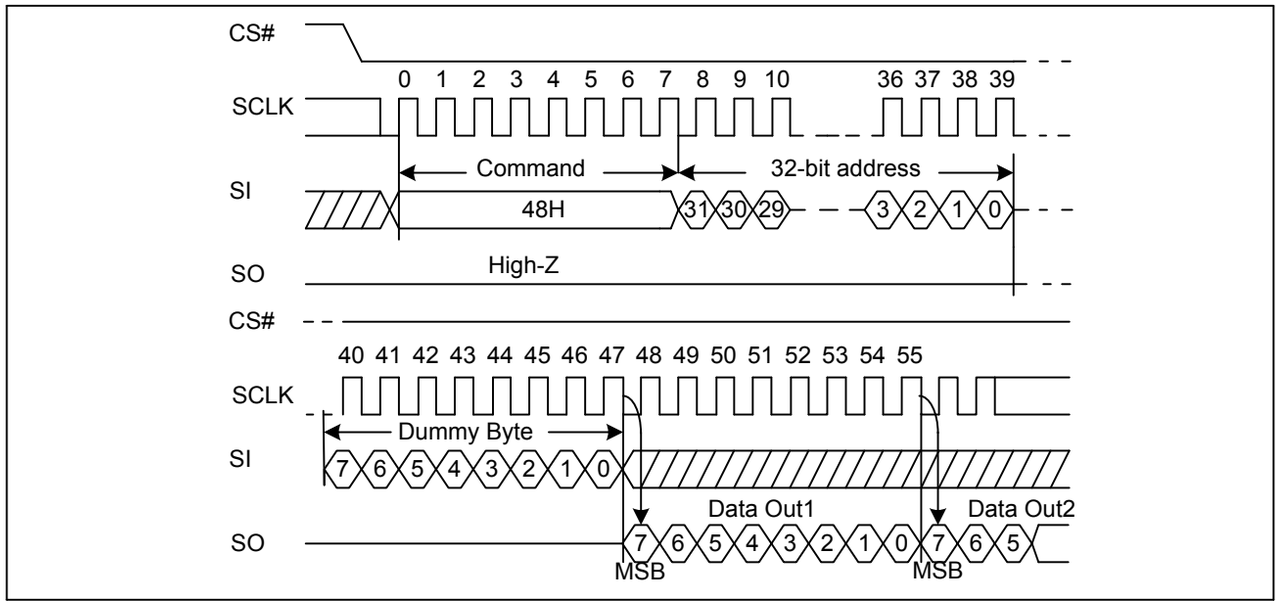



**Figure 77. Read Security Registers command Sequence Diagram (ADS=1)**

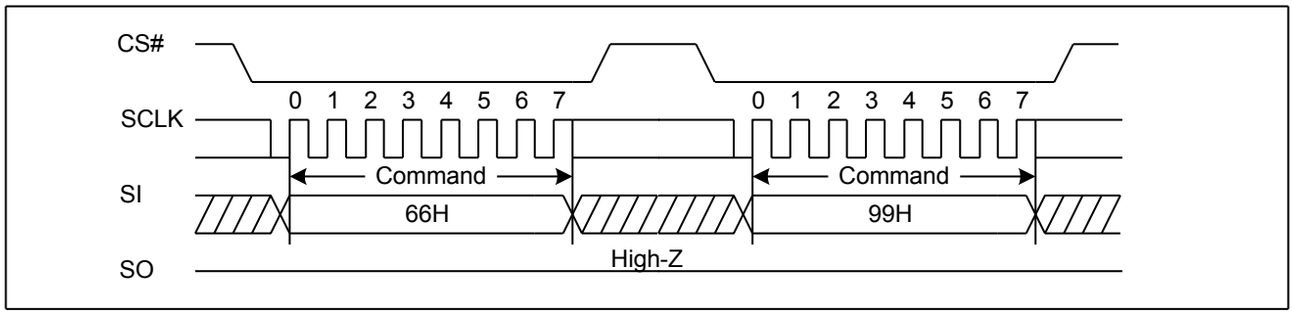


## 8.38. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in SPI mode. The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately $t_{RST}$ /$t_{RST\_E}$ to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

**Figure 78. Enable Reset and Reset command Sequence Diagram**




Note: Enable Reset (66H) and Reset (99H) commands have no effect when the device is in Quad I/O DTR Continuous Read Mode. The only way to quit the Quad I/O DTR Continuous Read Mode is to set the “Continuous Read Mode” bits (M5-4) not equal to (1,0).

## 8.39. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B.

**Figure 79. Read Serial Flash Discoverable Parameter command Sequence Diagram**

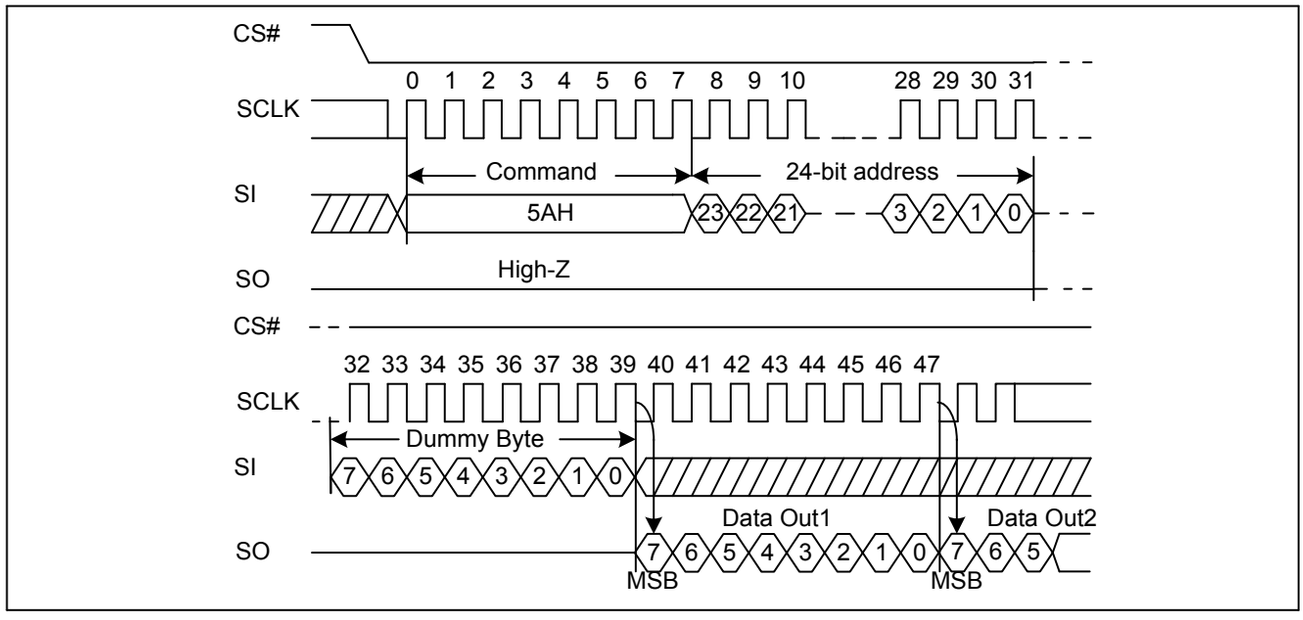


**Table 20. Signature and Parameter Identification Data Values**

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| SFDP Signature | Fixed:50444653H | 00H | 07:00 | 53H | 53H |
| | | 01H | 15:08 | 46H | 46H |
| | | 02H | 23:16 | 44H | 44H |
| | | 03H | 31:24 | 50H | 50H |
| SFDP Minor Revision Number | Start from 00H | 04H | 07:00 | 06H | 06H |
| SFDP Major Revision Number | Start from 01H | 05H | 15:08 | 01H | 01H |
| Number of Parameters Headers | Start from 00H | 06H | 23:16 | 02H | 02H |
| Unused | Contains 0xFFH and can never be changed | 07H | 31:24 | FFH | FFH |
| ID number (JEDEC) | 00H: It indicates a JEDEC specified header | 08H | 07:00 | 00H | 00H |
| Parameter Table Minor Revision Number | Start from 0x00H | 09H | 15:08 | 06H | 06H |
| Parameter Table Major Revision Number | Start from 0x01H | 0AH | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 0BH | 31:24 | 10H | 10H |
| Parameter Table Pointer (PTP) | First address of JEDEC Flash Parameter table | 0CH | 07:00 | 30H | 30H |
| | | 0DH | 15:08 | 00H | 00H |
| | | 0EH | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 0FH | 31:24 | FFH | FFH |
| ID Number (GigaDevice Manufacturer ID) | It is indicates GigaDevice manufacturer ID | 10H | 07:00 | C8H | C8H |
| Parameter Table Minor Revision Number | Start from 0x00H | 11H | 15:08 | 00H | 00H |
| Parameter Table Major Revision Number | Start from 0x01H | 12H | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 13H | 31:24 | 03H | 03H |
| Parameter Table Pointer (PTP) | First address of GigaDevice Flash Parameter table | 14H | 07:00 | 90H | 90H |
| | | 15H | 15:08 | 00H | 00H |
| | | 16H | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 17H | 31:24 | FFH | FFH |
| ID Number (4-Byte Address Instruction) | 4-Byte address instruction parameter ID | 18H | 07:00 | 84H | 84H |
| Parameter Table Minor Revision Number | Start from 0x00H | 19H | 15:08 | 00H | 00H |

| | | | | | |
|---|---|---|---|---|---|
| Parameter Table Major Revision Number | Start from 0x01H | 1AH | 23:16 | 01H | 01H |
| Parameter Table Length (in double word) | How many DWORDs in the Parameter table | 1BH | 31:24 | 02H | 02H |
| Parameter Table Pointer (PTP) | First address of GigaDevice Flash Parameter table | 1CH | 07:00 | C0H | C0H |
| | | 1DH | 15:08 | 00H | 00H |
| | | 1EH | 23:16 | 00H | 00H |
| Unused | Contains 0xFFH and can never be changed | 1FH | 31:24 | FFH | FFH |

**Table 21. Parameter Table (0): JEDEC Flash Parameter Tables**

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| Block/Sector Erase Size | 00: Reserved; 01: 4KB erase;<br>10: Reserved;<br>11: not support 4KB erase | 30H | 01:00 | 01b | E5H |
| Write Granularity | 0: 1Byte, 1: 64Byte or larger | | 02 | 1b | |
| Write Enable Instruction Requested for Writing to Volatile Status Registers | 0: Nonvolatile status bit<br>1: Volatile status bit<br>(BP status register bit) | | 03 | 0b | |
| Write Enable Opcode Select for Writing to Volatile Status Registers | 0: Use 50H Opcode,<br>1: Use 06H Opcode,<br>Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b. | | 04 | 0b | |
| Unused | Contains 111b and can never be changed | | 07:05 | 111b | |
| 4KB Erase Opcode | | 31H | 15:08 | 20H | 20H |
| (1-1-2) Fast Read | 0=Not support, 1=Support | 32H | 16 | 1b | FBH |
| Address Bytes Number used in addressing flash array | 00: 3Byte only, 01: 3 or 4Byte,<br>10: 4Byte only, 11: Reserved | | 18:17 | 01b | |
| Double Transfer Rate (DTR) clocking | 0=Not support, 1=Support | | 19 | 1b | |
| (1-2-2) Fast Read | 0=Not support, 1=Support | | 20 | 1b | |
| (1-4-4) Fast Read | 0=Not support, 1=Support | | 21 | 1b | |
| (1-1-4) Fast Read | 0=Not support, 1=Support | | 22 | 1b | |
| Unused | | | 23 | 1b | |
| Unused | | 33H | 31:24 | FFH | FFH |
| Flash Memory Density | | 37H:34H | 31:00 | 0FFFFFFFH (256Mb) | |
| (1-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 38H | 04:00 | 00100b | 44H |
| (1-4-4) Fast Read Number of Mode Bits | 000b:Mode Bits not support | | 07:05 | 010b | |
| (1-4-4) Fast Read Opcode | | 39H | 15:08 | EBH | EBH |
| (1-1-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3AH | 20:16 | 01000b | 08H |
| (1-1-4) Fast Read Number of Mode Bits | 000b:Mode Bits not support | | 23:21 | 000b | |
| (1-1-4) Fast Read Opcode | | 3BH | 31:24 | 6BH | 6BH |

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| (1-1-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3CH | 04:00 | 01000b | 08H |
| (1-1-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 07:05 | 000b | |
| (1-1-2) Fast Read Opcode | | 3DH | 15:08 | 3BH | 3BH |
| (1-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 3EH | 20:16 | 00010b | 42H |
| (1-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 010b | |
| (1-2-2) Fast Read Opcode | | 3FH | 31:24 | BBH | BBH |
| (2-2-2) Fast Read | 0=not support 1=support | 40H | 00 | 0b | EEH |
| Unused | | | 03:01 | 111b | |
| (4-4-4) Fast Read | 0=not support 1=support | | 04 | 0b | |
| Unused | | | 07:05 | 111b | |
| Unused | | 43H:41H | 31:08 | 0xFFH | 0xFFH |
| Unused | | 45H:44H | 15:00 | 0xFFH | 0xFFH |
| (2-2-2) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 46H | 20:16 | 00000b | 00H |
| (2-2-2) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (2-2-2) Fast Read Opcode | | 47H | 31:24 | FFH | FFH |
| Unused | | 49H:48H | 15:00 | 0xFFH | 0xFFH |
| (4-4-4) Fast Read Number of Wait states | 0 0000b: Wait states (Dummy Clocks) not support | 4AH | 20:16 | 00000b | 00H |
| (4-4-4) Fast Read Number of Mode Bits | 000b: Mode Bits not support | | 23:21 | 000b | |
| (4-4-4) Fast Read Opcode | | 4BH | 31:24 | FFH | FFH |
| Sector Type 1 Size | Sector/block size=2^N Bytes<br>0x00b: this sector type don't exist | 4CH | 07:00 | 0CH | 0CH |
| Sector Type 1 erase Opcode | | 4DH | 15:08 | 20H | 20H |
| Sector Type 2 Size | Sector/block size=2^N Bytes<br>0x00b: this sector type don't exist | 4EH | 23:16 | 0FH | 0FH |
| Sector Type 2 erase Opcode | | 4FH | 31:24 | 52H | 52H |
| Sector Type 3 Size | Sector/block size=2^N Bytes<br>0x00b: this sector type don't exist | 50H | 07:00 | 10H | 10H |
| Sector Type 3 erase Opcode | | 51H | 15:08 | D8H | D8H |
| Sector Type 4 Size | Sector/block size=2^N Bytes<br>0x00b: this sector type don't exist | 52H | 23:16 | 00H | 00H |
| Sector Type 4 erase Opcode | | 53H | 31:24 | FFH | FFH |

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| Multiplier from typical erase time to maximum erase time | | 54H | 3:0 | 0010b | 42H |
| Erase Type 1 Erase, Typical time | Erase time=70ms/80ms | | 7:4 | 0100b | |
| Erase Type 2 Erase, Typical time | Erase time=200ms/208ms | 55H | 10:8 | 010b | 62H |
| | | | 15:11 | 01100b | |
| Erase Type 3 Erase, Typical time | Erase time=300ms/304ms | 56H | 17:16 | 01b | C9H |
| | | | 23:18 | 110010b | |
| Erase Type 4 Erase, Typical time | Not exist | 57H | 24 | 0b | FEH |
| | | | 31:25 | 1111111b | |
| Multiplier from typical time to max time for Page or Byte program | | 58H | 3:0 | 0010b | 82H |
| Page Size | Page size=256Byte | | 7:4 | 1000b | |
| Page Program Typical time | Page program=600us/640us | 59H | 13:8 | 101001b | E9H |
| Byte Program Typical time, first Byte | First Byte program=30us/32us | | 15:14 | 11b | |
| Byte Program Typical time, additional Byte | Additional Byte program=2.5us/3us | 5AH | 18:16 | 100b | 14H |
| | | | 23:19 | 00010b | |
| Chip Erase, Typical time | Chip erase typical time=100s/100s | 5BH | 30:24 | 1011000b | 58H |
| Reserved | | | 31 | 0b | |
| Prohibited Operations During Program Suspend | | 5CH | 3:0 | 1100b | ECH |
| Prohibited Operations During Erase Suspend | | | 7:4 | 1110b | |
| Reserved | | 5DH | 8 | 0b | 60H |
| Program Resume to Suspend Interval | Interval=64us | | 12:9 | 0000b | |
| Suspend in-progress program max latency | max latency=20us/20us | | 15:13 | 011b | |
| | | 5EH | 19:16 | 0110b | 06H |
| Erase Resume to Suspend Interval | Interval=64us | | 23:20 | 0000b | |
| Suspend in-progress erase max latency | max latency=20us/20us | 5FH | 30:24 | 0110011b | 33H |
| Suspend / Resume supported | | | 31 | 0b | |
| Program Resume Instruction | | 60H | 7:0 | 7AH | 7AH |
| Program Suspend Instruction | | 61H | 15:0 | 75H | 75H |
| Resume Instruction | | 62H | 23:16 | 7AH | 7AH |
| Suspend Instruction | | 63H | 31:24 | 75H | 75H |

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| Reserved | | 64H | 1:0 | 00b | 04H |
| Status Register Polling Device Busy | Use of legacy polling is supported by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy). | | 7:2 | 000001b | |
| Exit Deep Power down to next operation delay | Delay=30us/30us | 65H | 14:8 | 0111101b | BDH |
| Exit Deep Power down Instruction | | | 15 | 1b | |
| Enter Deep Power down Instruction | | 66H | 22:16 | 1010101b | D5H |
| | | | 23 | 1b | |
| Deep Power down Supported | | 67H | 30:24 | 1011100b | 5CH |
| | | | 31 | 0b | |
| 4-4-4 mode disable sequences | Not support 4-4-4 mode | 68H | 3:0 | 0000b | 00H |
| 4-4-4 mode enable sequences | Not support 4-4-4 mode | | 7:4 | 000b | |
| 0-4-4 mode supported | Supported | 69H | 8 | 0b | 06H |
| | | | 9 | 1b | |
| 0-4-4 Mode Exit Method | M<7:0>=00H | | 15:10 | 000001b | |
| 0-4-4 Mode Entry Method | M<7:0>=AXH | 6AH | 19:16 | 0100b | 44H |
| Quad Enable Requirements (QER) | QE is in status register 2, bit 1 | | 22:20 | 100b | |
| RESET Disable | | | 23 | 0b | |
| Reserved | | 6BH | 31:24 | 00000000b | 00H |
| Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 | | 6CH | 6:0 | 0001000b | 08H |
| Reserved | | | 7 | 0b | |
| Soft Reset and Rescue Sequence Support | 66H-99H | 6DH | 13:8 | 010000b | 50H |
| Exit 4-Byte Addressing | | | 15:14 | 01b | |
| | | 6EH | 23:16 | 00000000b | 00H |
| Enter 4-Bye Addressing | | 6FH | 31:24 | 00000001b | 01H |

Note:

1. All AC/DC characteristics related content in SFDP applies to -40℃~85℃ products only.

**Table 22. Parameter Table (1): GigaDevice Flash Parameter Tables**

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| Vcc Supply Maximum Voltage | 2000H=2.000V<br>2700H=2.700V<br>3600H=3.600V | 91H:90H | 15:00 | 3600H | 3600H |
| Vcc Supply Minimum Voltage | 1650H=1.650V<br>2250H=2.250V<br>2350H=2.350V<br>2700H=2.700V | 93H:92H | 31:16 | 2700H | 2700H |
| HW Reset# pin | 0=not support 1=support | 95H:94H | 00 | 0b(1) | F99CH |
| HW Hold# pin | 0=not support 1=support | | 01 | 0b | |
| Deep Power Down Mode | 0=not support 1=support | | 02 | 1b | |
| SW Reset | 0=not support 1=support | | 03 | 1b | |
| SW Reset Opcode | Should be issue Reset Enable(66H) before Reset cmd. | | 11:04 | 1001 1001b (99H) | |
| Program Suspend/Resume | 0=not support 1=support | | 12 | 1b | |
| Erase Suspend/Resume | 0=not support 1=support | | 13 | 1b | |
| Unused | | | 14 | 1b | |
| Wrap-Around Read mode | 0=not support 1=support | | 15 | 1b | |
| Wrap-Around Read mode Opcode | | 96H | 23:16 | 77H | 77H |
| Wrap-Around Read data length | 08H:support 8B wrap-around read<br>16H:8B&16B<br>32H:8B&16B&32B<br>64H:8B&16B&32B&64B | 97H | 31:24 | 64H | 64H |
| Individual block lock | 0=not support 1=support | 9BH:98H | 00 | 0b | CBFCH |
| Individual block lock bit (Volatile/Nonvolatile) | 0=Volatile 1=Nonvolatile | | 01 | 0b | |
| Individual block lock Opcode | | | 09:02 | FFH | |
| Individual block lock Volatile protect bit default protect status | 0=protect 1=unprotect | | 10 | 0b | |
| Secured OTP | 0=not support 1=support | | 11 | 1b | |
| Read Lock | 0=not support 1=support | | 12 | 0b | |
| Permanent Lock | 0=not support 1=support | | 13 | 0b | |
| Unused | | | 15:14 | 11b | |
| Unused | | | 31:16 | FFFFH | FFFFH |

NOTE:

1. GD25B257DxxRx of the SOP16 and TFBGA packages, a dedicated RESET# pin is provided.

**Table 23. Parameter Table (2): 4-Byte Instruction Tables**

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| Support for (1-1-1) READ command. Instruction = 13H | 0 = NOT supported<br>1 = supported | C0H | 00 | 1b | FFH |
| Support for (1-1-1) FAST READ command. Instruction = 0CH | 0 = NOT supported<br>1 = supported | | 01 | 1b | |
| Support for (1-1-2) FAST READ command. Instruction = 3CH | 0 = NOT supported<br>1 = supported | | 02 | 1b | |
| Support for (1-2-2) FAST READ command. Instruction = BCH | 0 = NOT supported<br>1 = supported | | 03 | 1b | |
| Support for (1-1-4) FAST READ command. Instruction = 6CH | 0 = NOT supported<br>1 = supported | | 04 | 1b | |
| Support for (1-4-4) FAST READ command. Instruction = ECH | 0 = NOT supported<br>1 = supported | | 05 | 1b | |
| Support for (1-1-1) Page Program command. Instruction = 12H | 0 = NOT supported<br>1 = supported | | 06 | 1b | |
| Support for (1-1-4) Page Program command. Instruction = 34H | 0 = NOT supported<br>1 = supported | | 07 | 1b | |
| Support for (1-4-4) Page Program command. Instruction = 3EH | 0 = NOT supported<br>1 = supported | C1H | 08 | 0b | 8EH |
| Support for Erase Command - Type 1 size. Instruction lookup in next the dword | 0 = NOT supported<br>1 = supported | | 09 | 1b | |
| Support for Erase Command - Type 2 size. Instruction lookup in next the dword | 0 = NOT supported<br>1 = supported | | 10 | 1b | |
| Support for Erase Command - Type 3 size. Instruction lookup in next the dword | 0 = NOT supported<br>1 = supported | | 11 | 1b | |
| Support for Erase Command - Type 4 size. Instruction lookup in next the dword | 0 = NOT supported<br>1 = supported | | 12 | 0b | |
| Support for (1-1-1) DTR READ command. Instruction = 0EH | 0 = NOT supported<br>1 = supported | | 13 | 0b | |
| Support for (1-2-2) DTR READ command. Instruction = BEH | 0 = NOT supported<br>1 = supported | | 14 | 0b | |
| Support for (1-4-4) DTR READ command. Instruction = EEH | 0 = NOT supported<br>1 = supported | | 15 | 1b | |

| Description | Comment | Add(H) (Byte) | DW Add (Bit) | Data | Data |
|---|---|---|---|---|---|
| Support for volatile individual sector lock Read command. Instruction = E0H | 0 = NOT supported<br>1 = supported | C2H | 16 | 0b | F0H |
| Support for volatile individual sector lock Write command. Instruction = E1H | 0 = NOT supported<br>1 = supported | | 17 | 0b | |
| Support for non-volatile individual sector lock Read command. Instruction = E2H | 0 = NOT supported<br>1 = supported | | 18 | 0b | |
| Support for non-volatile individual sector lock Write command. Instruction = E3H | 0 = NOT supported<br>1 = supported | | 19 | 0b | |
| Reserved | Reserved | | 23:20 | 1111b | |
| Reserved | Reserved | C3H | 31:24 | FFH | FFH |
| Instruction for Erase Type 1 | FFH = NOT supported | C4H | 07:00 | 21H | 21H |
| Instruction for Erase Type 2 | FFH = NOT supported | C5H | 15:08 | 5CH | 5CH |
| Instruction for Erase Type 3 | FFH = NOT supported | C6H | 23:16 | DCH | DCH |
| Instruction for Erase Type 4 | FFH = NOT supported | C7H | 31:24 | FFH | FFH |

# 9. ELECTRICAL CHARACTERISTICS

## 9.1. POWER-ON TIMING

**Figure 80.Power-on Timing**

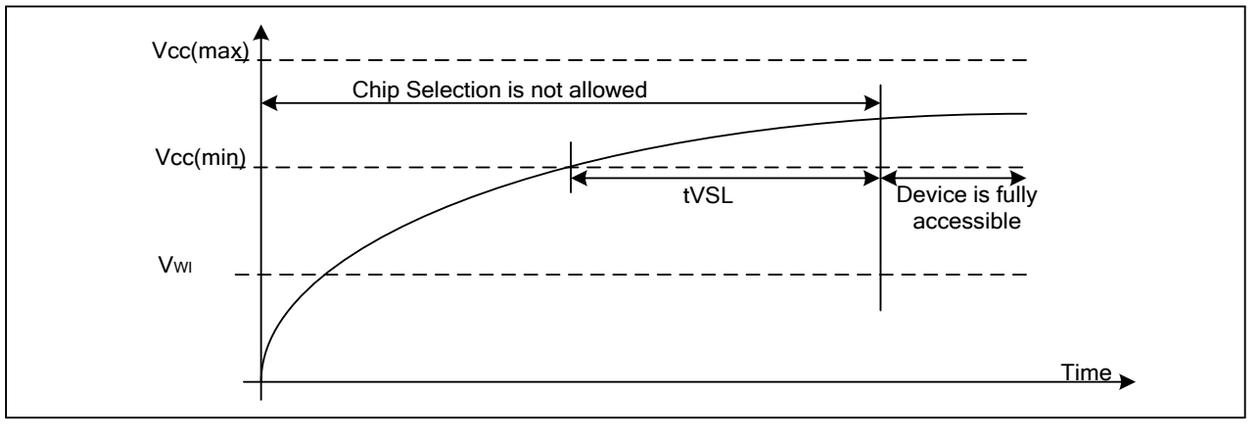



**Table 24. Power-Up Timing and Write Inhibit Threshold**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| tVSL | VCC (min) To CS# Low | 2.5 | | ms |
| VWI | Write Inhibit Voltage | 1.5 | 2.5 | V |

## 9.2. INITIAL DELIVERY STATE

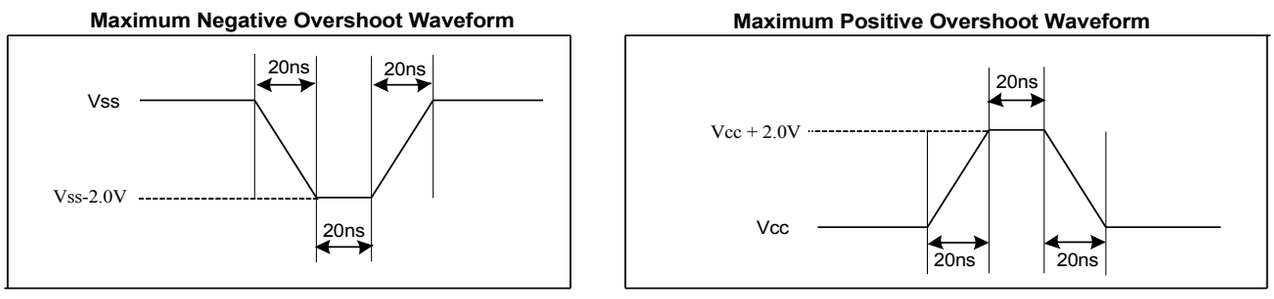
The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register bits are set to 0, except QE bit (S9) and DRV0 bit (S21) are set to 1.

## 9.3. ABSOLUTE MAXIMUM RATINGS

**Table 25. Absolute Maximum Ratings**

| Parameter | Value | Unit |
|---|---|---|
| Ambient Operating Temperature | -40 to 85 | ℃ |
| Storage Temperature | -65 to 150 | ℃ |
| Applied Input/Output Voltage | -0.6 to VCC+0.4 | V |
| Transient Input/Output Voltage (**note:** overshoot) | -2.0 to VCC+2.0 | V |
| VCC | -0.6 to 4.2 | V |

**Figure 81. Input Test Waveform and Measurement Level**

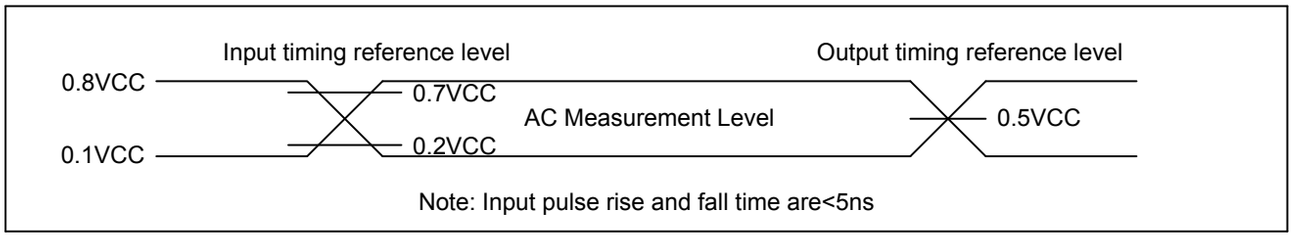


## 9.4. CAPACITANCE MEASUREMENT CONDITIONS

**Table 26. Capacitance Measurement Conditions**

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | 6 | pF | VIN=0V |
| COUT | Output Capacitance | | | 8 | pF | VOUT=0V |
| $C_L$ | Load Capacitance | | 30 | | pF | |
| | Input Rise And Fall time | | | 5 | ns | |
| | Input Pulse Voltage | 0.1VCC to 0.8VCC | | | V | |
| | Input Timing Reference Voltage | 0.2VCC to 0.7VCC | | | V | |
| | Output Timing Reference Voltage | 0.5VCC | | | V | |

**Figure 82. Input/Output Timing Reference Level**



## 9.5. DC CHARACTERISTICS

(T= -40℃~85℃, VCC=2.7~3.6V)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | | | | ±2 | μA |
| $I_{LO}$ | Output Leakage Current | | | | ±2 | μA |
| $I_{CC1}$ | Standby Current | CS#=VCC, $V_{IN}$=VCC or VSS | | 12 | 50 | μA |
| $I_{CC2}$ | Deep Power-Down Current | CS#=VCC, $V_{IN}$=VCC or VSS | | 1 | 8 | μA |
| $I_{CC3}$ | Operating Current (Read) | CLK=0.1VCC / 0.9VCC at 104MHz, Q=Open(*1,*2,*4 I/O) | | 15 | 25 | mA |
| | | CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O) | | 13 | 20 | mA |
| | | CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*4 I/O DTR) | | 16 | 25 | mA |
| $I_{CC4}$ | Operating Current (PP) | CS#=VCC | | | 25 | mA |
| $I_{CC5}$ | Operating Current (WRSR) | CS#=VCC | | | 25 | mA |
| $I_{CC6}$ | Operating Current (SE) | CS#=VCC | | | 25 | mA |
| $I_{CC7}$ | Operating Current (BE) | CS#=VCC | | | 25 | mA |
| $I_{CC8}$ | Operating Current (CE) | CS#=VCC | | | 25 | mA |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.2VCC | V |
| $V_{IH}$ | Input High Voltage | | 0.7VCC | | VCC+0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ =100μA | | | 0.2 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ =-100μA | VCC-0.2 | | | V |

Note:

1. Typical value tested at T = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

## 9.6. AC CHARACTERISTICS

(T= -40℃~85℃, VCC=2.7~3.6V, CL=30pf)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{C0}$ | Serial Clock Frequency for all instructions except Read | | | 104 | MHz |
| $f_{C1}$ | Serial Clock Frequency for Dual I/O (BBH, BCH), Quad I/O (EBH, ECH), Dual Output (3BH, 3CH), Quad Output (6BH, 6CH), Fast Read (0BH, 0CH) instructions, on 3.0 - 3.6V power supply | | | 104 | MHz |
| $f_{C2}$ | Serial Clock Frequency for DTR Quad I/O Fast Read (EEH, EDH) instructions, on 3.0 - 3.6V power supply | | | 80 | MHz |
| $f_{C3}$ | Serial Clock Frequency for Dual I/O (BBH, BCH), Quad I/O (EBH, ECH), Dual Output (3BH, 3CH), Quad Output (6BH, 6CH), Fast Read (0BH, 0CH) instructions, on 2.7 – 3.0V power supply | | | 80 | MHz |
| $f_{C4}$ | Serial Clock Frequency for DTR Quad I/O Fast Read (EEH, EDH) instructions, on 2.7 – 3.0V power supply | | | 70 | MHz |
| $f_R$ | Serial Clock Frequency For: Read (03H, 13H) | | | 50 | MHz |
| $t_{CLH1}$ | Serial Clock High Time in STR Mode | 3.7 | | | ns |
| $t_{CLH2}$ | Serial Clock High Time in DTR Mode | 5.6 | | | ns |
| $t_{CLL1}$ | Serial Clock Low Time in STR Mode | 3.7 | | | ns |
| $t_{CLL2}$ | Serial Clock Low Time in DTR Mode | 5.6 | | | ns |
| $t_{CLCH}$ | Serial Clock Rise Time (Slew Rate) | 0.2 | | | V/ns |
| $t_{CHCL}$ | Serial Clock Fall Time (Slew Rate) | 0.2 | | | V/ns |
| $t_{SLCH}$ | CS# Active Setup Time | 8 | | | ns |
| $t_{CHSH}$ | CS# Active Hold Time | 5 | | | ns |
| $t_{SHCH}$ | CS# Not Active Setup Time | 5 | | | ns |
| $t_{CHSL}$ | CS# Not Active Hold Time | 5 | | | ns |
| $t_{SHSL}$ | CS# High Time (Read/Write) | 20 | | | ns |
| $t_{SHQZ}$ | Output Disable Time | | | 6 | ns |
| $t_{CLQX}$ | Output Hold Time | 1.8 | | | ns |
| $t_{DVCH}$ | Data In Setup Time | 2 | | | ns |
| $t_{CHDX}$ | Data In Hold Time | 2 | | | ns |
| $t_{CLQV}$ | Clock Low To Output Valid | | | 7 | ns |
| $t_{DP}$ | CS# High To Deep Power-Down Mode | | | 20 | μs |
| $t_{RES1}$ | CS# High To Standby Mode Without Electronic Signature Read | | | 30 | μs |
| $t_{RES2}$ | CS# High To Standby Mode With Electronic Signature Read | | | 30 | μs |
| $t_{SUS}$ | CS# High To Next Command After Suspend | | | 20 | μs |
| $t_{RS}$ | Latency Between Resume And Next Suspend | 100 | | | μs |
| $t_{RST}$ | CS# High To Next Command After Reset (Except From Erase) | | | 30 | us |
| $t_{RST\_E}$ | CS# High To Next Command After Reset (From Erase) | | | 12 | ms |
| $t_W$ | Write Status Register Cycle Time | | 5 | 20 | ms |
| $t_{BP1}$ | Byte Program Time (First Byte) | | 30 | 50 | μs |
| $t_{BP2}$ | Additional Byte Program Time (After First Byte) | | 2.5 | 12 | μs |

| | | | | | |
|---|---|---|---|---|---|
| $t_{PP}$ | Page Programming Time | | 0.4 | 2.4 | ms |
| $t_{SE}$ | Sector Erase Time | | 70 | 400 | ms |
| $t_{BE1}$ | Block Erase Time (32K Bytes) | | 0.16 | 0.8 | s |
| $t_{BE2}$ | Block Erase Time (64K Bytes) | | 0.22 | 1 | s |
| $t_{CE}$ | Chip Erase Time (GD25B257D) | | 70 | 200 | s |

Note:

1. Typical value tested at T = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

**Figure 83. Serial Input Timing**

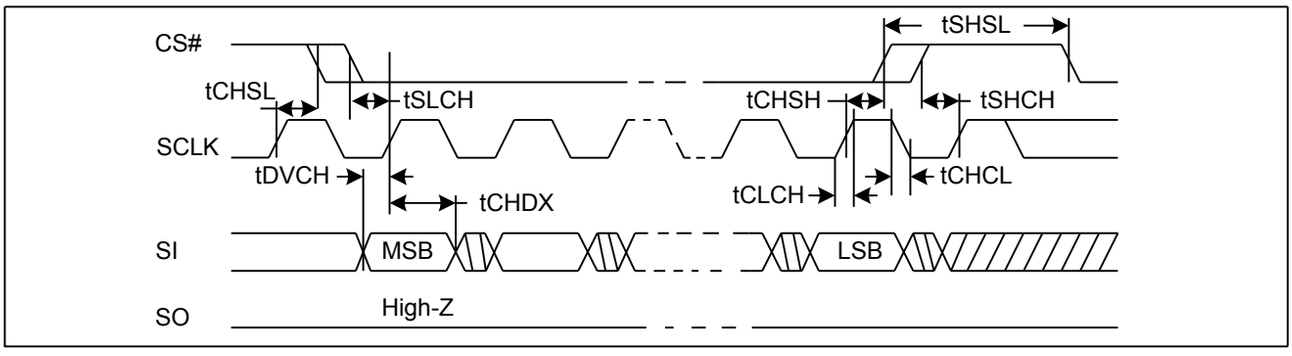



**Figure 84. Output Timing**

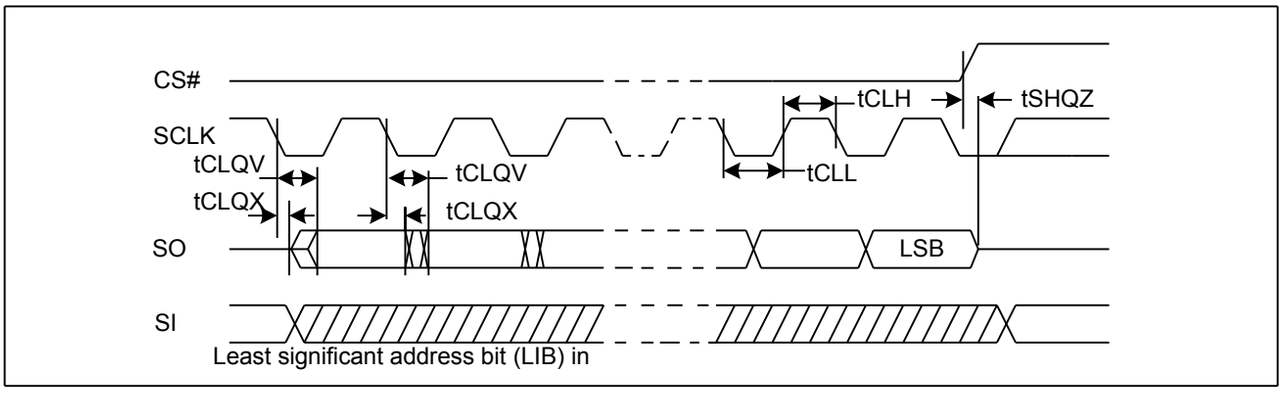


**Figure 85. Resume to Suspend Timing Diagram**

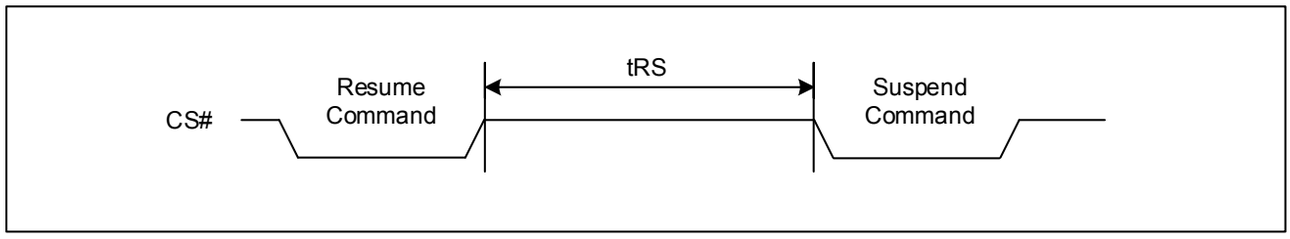



**Figure 86 RESET Timing**

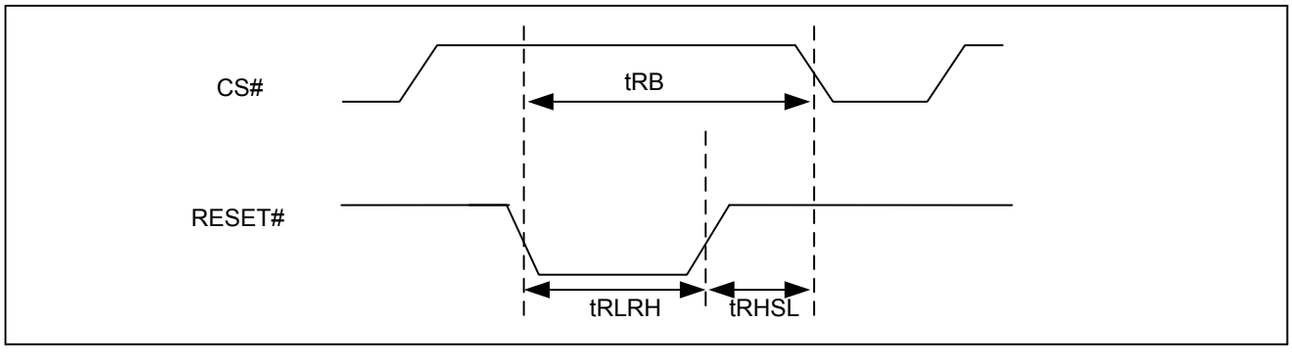
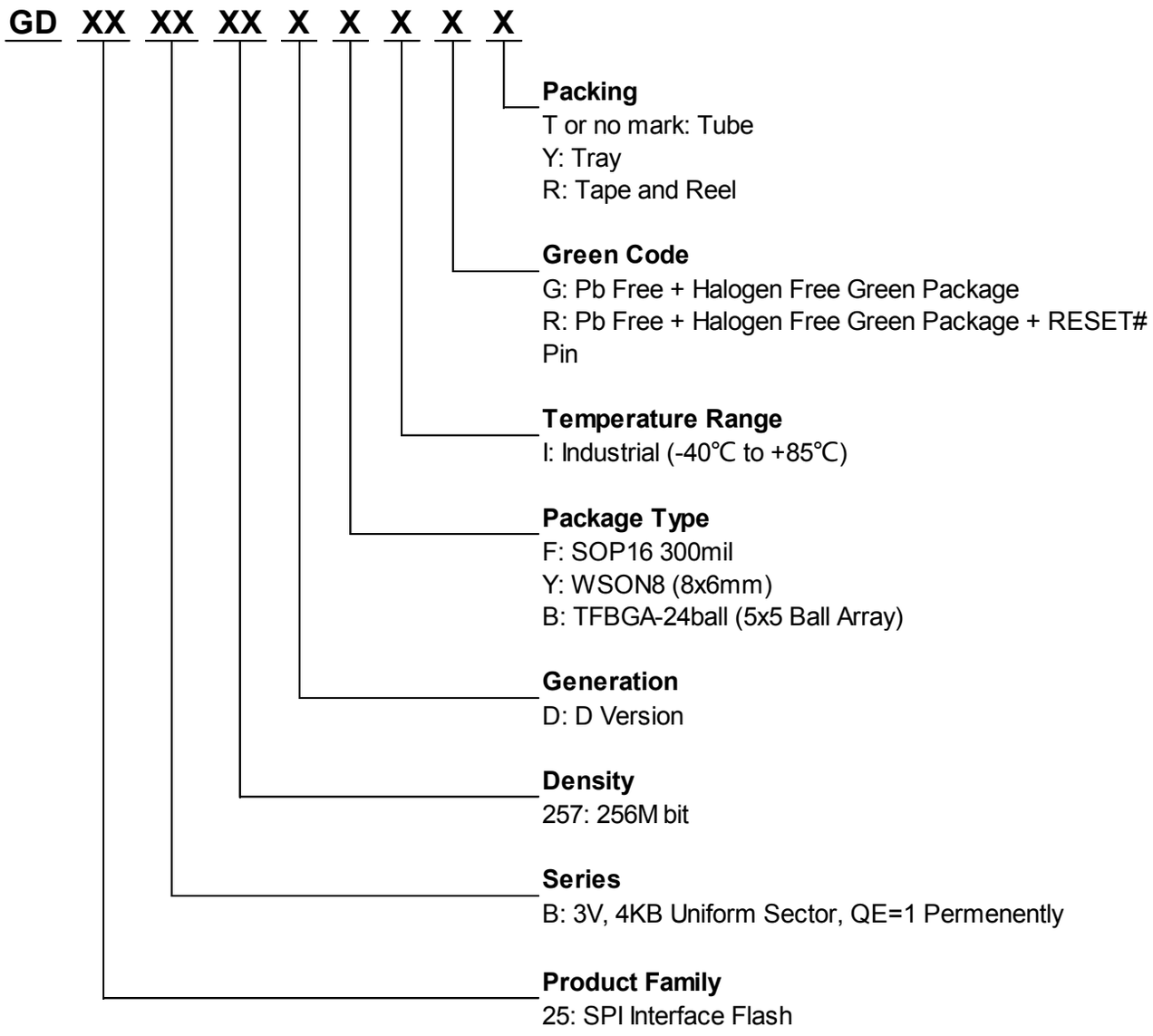



**Table 27. Reset Timing**

| Symbol | Parameter | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|
| tRLRH | Reset Pulse Width | 1 | | | μs |
| tRHSL | Reset High Time Before Read | 50 | | | ns |
| tRB | Reset Recovery Time | | | 12 | ms |

# 10. ORDERING INFORMATION



## 10.1. Valid Part Numbers

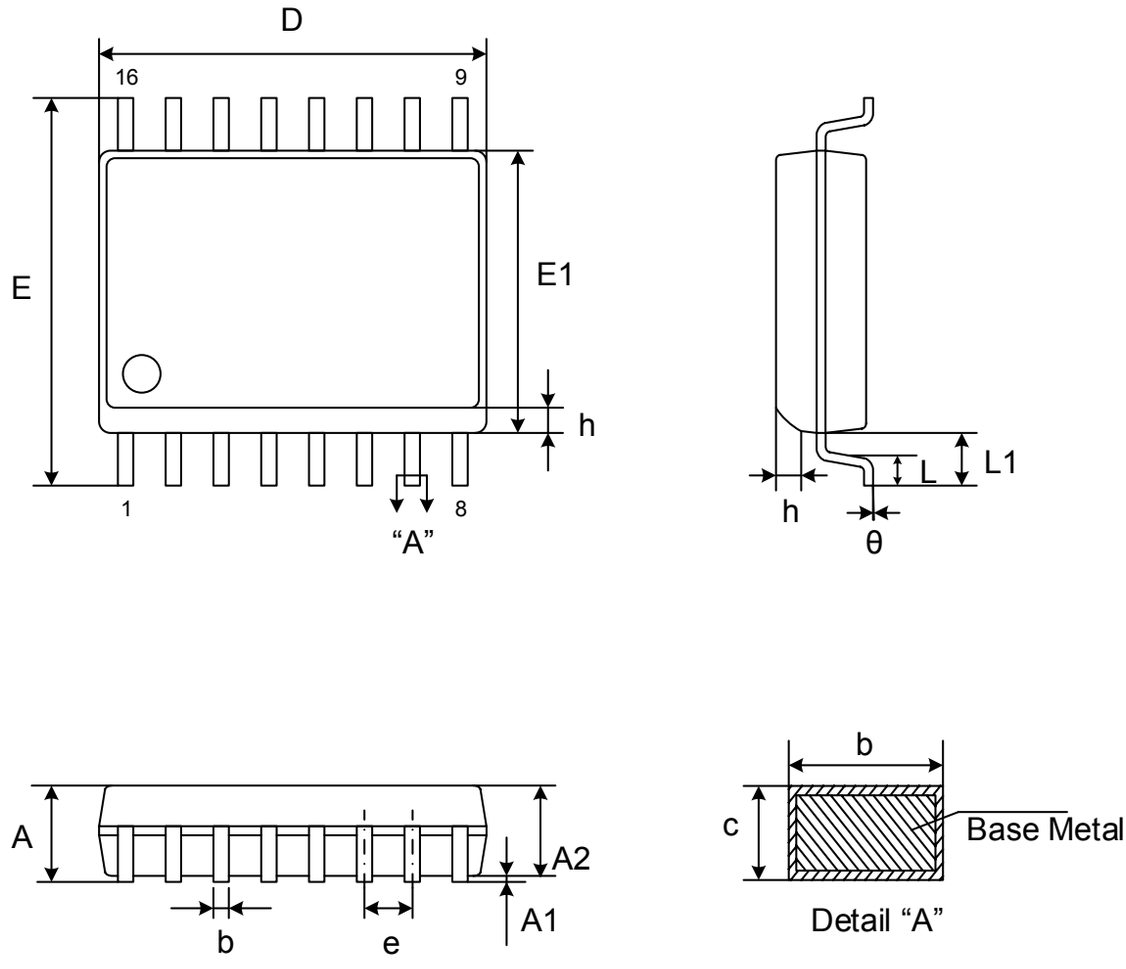
Please contact GigaDevice regional sales for the latest product selection and available form factors.

**Temperature Range I: Industrial (-40℃ to +85℃)**

| Product Number | Density | Package Type |
|---|---|---|
| GD25B257DFIG | 256Mbit | SOP16 300mil |
| GD25B257DFIR | | |
| GD25B257DYIG | 256Mbit | WSON8 (8*6mm) |
| GD25B257DBIG | 256Mbit | TFBGA-24ball (5*5 Ball Array) |
| GD25B257DBIR | | |

# 11. PACKAGE INFORMATION

## 11.1. Package SOP16 300MIL



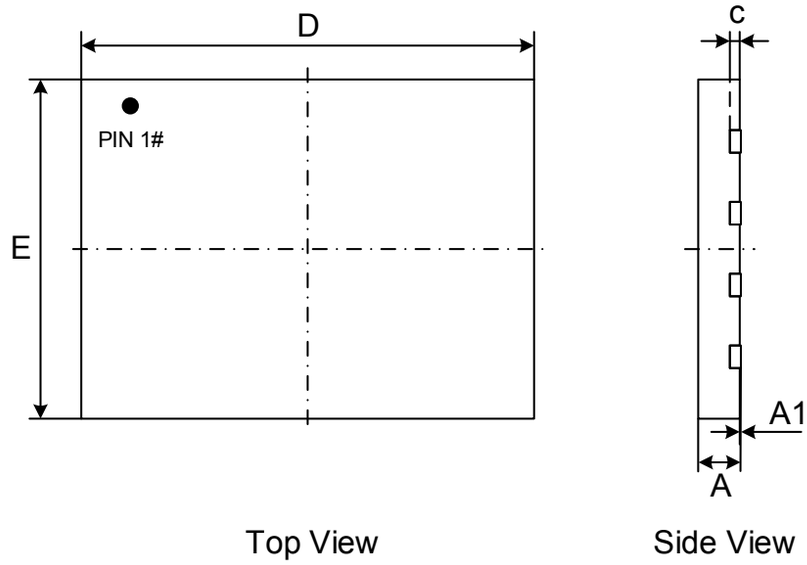

**Dimensions**

| Symbol / Unit | | A | A1 | A2 | b | c | D | E | E1 | e | L | L1 | h | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | - | 0.10 | 2.05 | 0.31 | 0.10 | 10.20 | 10.10 | 7.40 | 1.27 | 0.40 | 1.40 | 0.25 | 0 |
| | Nom | - | 0.20 | - | 0.41 | 0.25 | 10.30 | 10.30 | 7.50 | | - | | - | - |
| | Max | 2.65 | 0.30 | 2.55 | 0.51 | 0.33 | 10.40 | 10.50 | 7.60 | | 1.27 | | 0.75 | 8 |

Note:

1. Both the package length and width do not include the mold flash.
2. Seating plane: Max. 0.1mm.

## 11.2. Package WSON8 (8*6mm)



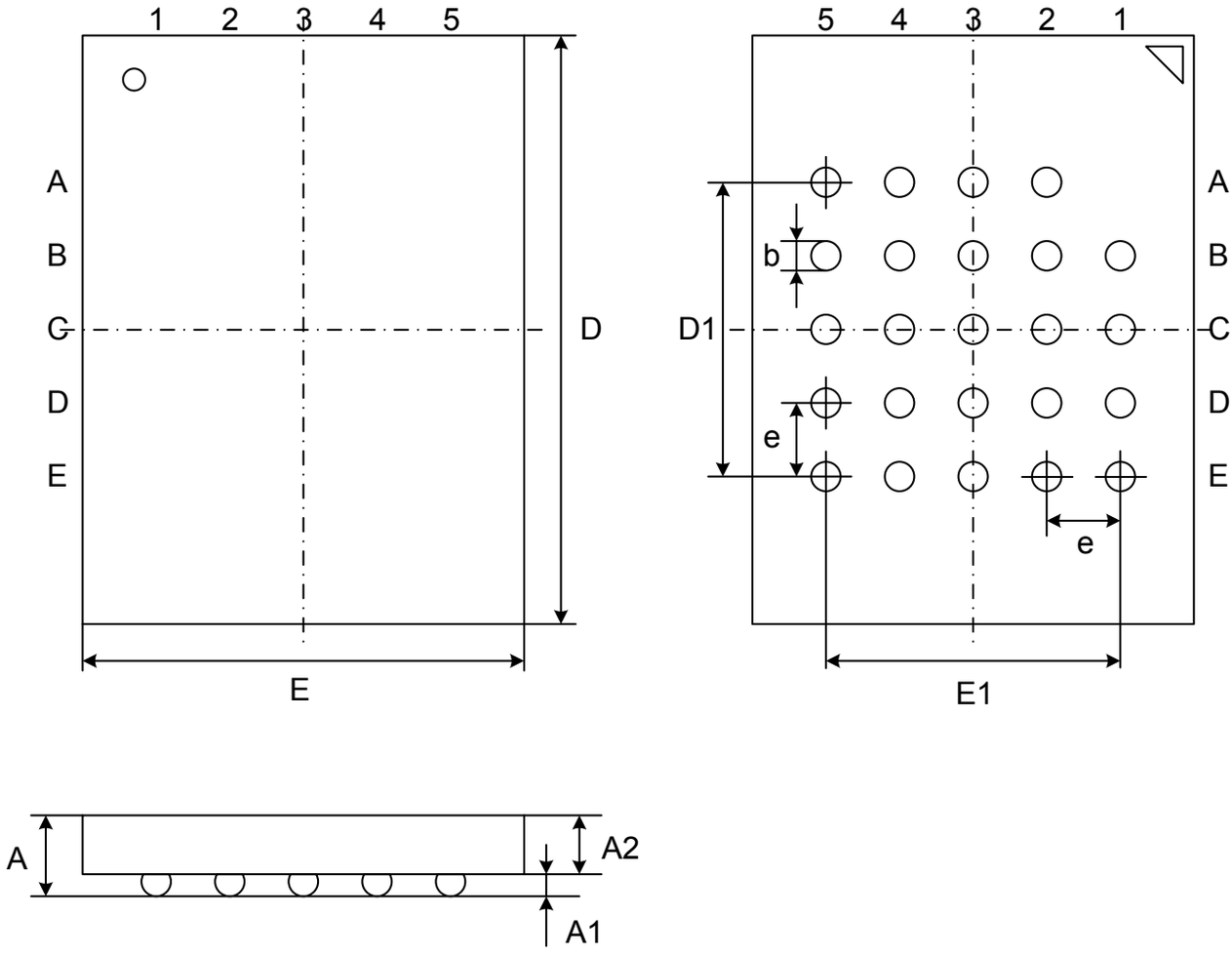

**Dimensions**

| Symbol / Unit | | A | A1 | c | b | D | D2 | E | E2 | e | L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | 0.70 | 0.00 | 0.180 | 0.35 | 7.90 | 3.30 | 5.90 | 4.20 | 1.27 | 0.45 |
| | Nom | 0.75 | 0.02 | 0.203 | 0.40 | 8.00 | 3.40 | 6.00 | 4.30 | | 0.50 |
| | Max | 0.80 | 0.05 | 0.250 | 0.45 | 8.10 | 3.50 | 6.10 | 4.40 | | 0.55 |

Note:

1. Both the package length and width do not include the mold flash.
2. The exposed metal pad area on the bottom of the package is floating.
3. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.
4. The lead shape may be of little difference according to different package lead frames. These lead shapes are compatible with each other.

## 11.3. Package TFBGA-24BALL (5*5 ball array)




**Dimensions**

| Symbol / Unit | | A | A1 | A2 | b | E | E1 | D | D1 | e |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | Min | - | 0.25 | 0.75 | 0.35 | 5.90 | 4.00 | 7.90 | 4.00 | 1.00 |
| | Nom | - | 0.30 | 0.80 | 0.40 | 6.00 | | 8.00 | | |
| | Max | 1.20 | 0.35 | 0.85 | 0.45 | 6.10 | | 8.10 | | |

Note: Both the package length and width do not include the mold flash.

# 12. REVISION HISTORY

| Version No. | Description | Page | Date |
|---|---|---|---|
| 1.0 | Initial Release | All | 2018-3-27 |
| 1.1 | Modify the Timing Diagrams of ED/EEH command<br>Modify tw typ. value from 1ms to 5ms | P42-44<br>P80 | 2018-5-2 |
| 1.2 | Modify Icc1 typ. value from 15uA to 12uA<br>AModify tPP typ. value from 0.6ms to 0.4ms<br>Modify tBE1 typ. value from 0.2s to 0.16s<br>Modify tBE2 typ. value from 0.3s to 0.22s<br>Modify tCE from 100-240s to 70-200s | P82<br>P84<br>P84<br>P84<br>P84 | 2018-7-9 |
| 1.3 | Modify the description of DRV bits<br>Add Icc3 in DTR mode | P14<br>P82 | 2019-4-17 |

# Important Notice

This document is the property of GigaDevice Semiconductor (Beijing) Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company under the intellectual property laws and treaties of the People’s Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as it’s suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as it’s suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products. Customers shall discard the device according to the local environmental law.

**Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Products and services described herein at any time, without notice.**