GD25B32C
DATASHEET

3.3V Uniform Sector Dual and Quad Serial Flash

GD25B32C

Content

1. FEATURES

- ♦ 32M-bit Serial Flash
  - -4096K-byte
  - -256 bytes per programmable page

- ♦ Standard, Dual, Quad SPI
  - -Standard SPI: SCLK, CS#, SI, SO
  - -Dual SPI: SCLK, CS#, IO0, IO1
  - -Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3

- ♦ High Speed Clock Frequency
  - -120MHz for fast read with 30PF load
  - -Dual I/O Data transfer up to 240Mbits/s
  - -Quad I/O Data transfer up to 480Mbits/s
  - -Continuous Read With 8/16/32/64-byte Wrap

- ♦ Software Write Protection
  - -Write protect all/portion of memory via software
  - -Top or Bottom, Sector or Block selection

- ♦ Cycling endurance
  - -Minimum 100,000 Program/Erase Cycles

- ♦ Data Retention
  - -20-year data retention typical

- ♦ Program/Erase Speed
  - -Page Program time: 0.6ms typical
  - -Sector Erase time: 50ms typical
  - -Block Erase time: 0.15/0.25s typical
  - -Chip Erase time: 15s typical

- ♦ Flexible Architecture
  - -Sector of 4K-byte
  - -Block of 32/64K-byte

- ♦ Low Power Consumption
  - -1μA typical stand-by active current
  - -1μA typical power down current

- ♦ Advanced Security Features
  - -128-bit Unique ID for each device
  - -3*1024-Byte Security Registers With OTP Locks
  - -Discoverable parameters (SFDP) register

- ♦ Single Power Supply Voltage
  - -Full voltage range: 2.7~3.6V

- ♦ Package Information
  - -SOP8 (208mil)
  - -DIP8 (300mil)
  - -USON8 3x4mm
  - -WSON8 (6*5mm)

2. GENERAL DESCRIPTION

The GD25B32C (32M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, and I/O3. The Dual I/O data is transferred with speed of 240Mbits/s and the Quad I/O & Quad output data is transferred with speed of 480Mbits/s.

CONNECTION DIAGRAM

8 - LEAD USON/WSON

8 - LEAD SOP/DIP
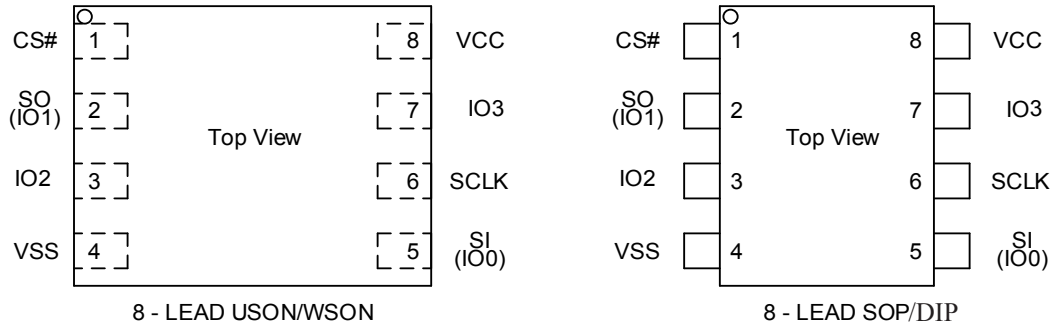
PIN DESCRIPTION

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
IO2	I/O	Data Input Output 2
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
IO3	I/O	Data Input Output 3
VCC		Power Supply

Note: CS# must be driven high if chip is not selected. Please don't leave CS# floating any time after power is on.

BLOCK DIAGRAM
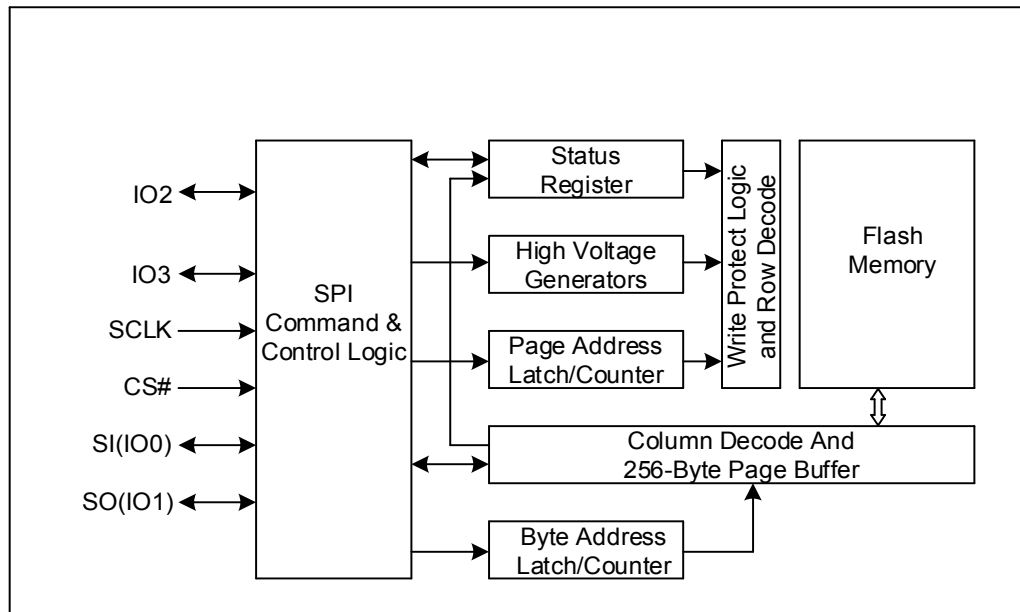
3. MEMORY ORGANIZATION

GD25B32C

Each device has	Each block has	Each sector has	Each page has	
4M	64/32K	4K	256	bytes
16K	256/128	16	-	pages
1024	16/8	-	-	sectors
64/128	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

GD25B32C 64K Bytes Block Sector Architecture

Block	Sector	Address range	
63	1023	3FF000H	3FFFFFH
	-----	-----	-----
	1008	3F0000H	3F0FFFH
62	1007	3EF000H	3EFFFFH
	-----	-----	-----
	992	3E0000H	3E0FFFH
-----	-----	-----	-----
	-----	-----	-----
	-----	-----	-----
-----	-----	-----	-----
	-----	-----	-----
	-----	-----	-----
2	47	02F000H	02FFFFH
	-----	-----	-----
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	-----	-----	-----
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	-----	-----	-----
	0	000000H	000FFFH

4. DEVICE OPERATION

SPI Mode

Standard SPI

The GD25B32C features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The GD25B32C supports Dual SPI operation when using the "Dual Output Fast Read" (3BH), "Dual I/O Fast Read" (BBH) and "Read Manufacture ID/ Device ID Dual I/O" (92H) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The GD25B32C supports Quad SPI operation when using the "Quad Output Fast Read"," Quad I/O Fast Read", "Quad I/O Word Fast Read" (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

5. DATA PROTECTION

The GD25B32C provide the following data protection methods:

♦ Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)

♦ Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits define the section of the memory array that can be read but not change.

♦ Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP0~1 bits.

♦ Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0 GD25B32C Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
×	×	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000H-3FFFFFH	64KB	Upper 1/64
0	0	0	1	0	62 to 63	3E0000H-3FFFFFH	128KB	Upper 1/32
0	0	0	1	1	60 to 63	3C0000H-3FFFFFH	256KB	Upper 1/16
0	0	1	0	0	56 to 63	380000H-3FFFFFH	512KB	Upper 1/8
0	0	1	0	1	48 to 63	300000H-3FFFFFH	1MB	Upper 1/4
0	0	1	1	0	32 to 63	200000H-3FFFFFH	2MB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/64
0	1	0	1	0	0 to 1	000000H-01FFFFH	128KB	Lower 1/32
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/16
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/8
0	1	1	0	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/4
0	1	1	1	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/2
×	×	1	1	1	0 to 63	000000H-3FFFFFH	4MB	ALL
1	0	0	0	1	63	3FF000H-3FFFFFH	4KB	Top Block
1	0	0	1	0	63	3FE000H-3FFFFFH	8KB	Top Block
1	0	0	1	1	63	3FC000H-3FFFFFH	16KB	Top Block
1	0	1	0	×	63	3F8000H-3FFFFFH	32KB	Top Block
1	0	1	1	0	63	3F8000H-3FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	×	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table1.1. GD25B32C Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
×	×	0	0	0	ALL	000000H-3FFFFFH	4MB	ALL
0	0	0	0	1	0 to 62	000000H-3EFFFFH	4032KB	Lower 63/64
0	0	0	1	0	0 to 61	000000H-3DFFFFH	3968KB	Lower 31/32
0	0	0	1	1	0 to 59	000000H-3BFFFFH	3840KB	Lower 15/16
0	0	1	0	0	0 to 55	000000H-37FFFFH	3584KB	Lower 7/8
0	0	1	0	1	0 to 47	000000H-2FFFFFH	3MB	Lower 3/4
0	0	1	1	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/2
0	1	0	0	1	1 to 63	010000H-3FFFFFH	4032KB	Upper 63/64
0	1	0	1	0	2 to 63	020000H-3FFFFFH	3968KB	Upper 31/32
0	1	0	1	1	4 to 63	040000H-3FFFFFH	3840KB	Upper 15/16
0	1	1	0	0	8 to 63	080000H-3FFFFFH	3584KB	Upper 7/8
0	1	1	0	1	16 to 63	100000H-3FFFFFH	3MB	Upper 3/4
0	1	1	1	0	32 to 63	200000H-3FFFFFH	2MB	Upper 1/2
×	×	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 63	000000H-3FEFFFH	4092KB	L-1023/1024
1	0	0	1	0	0 to 63	000000H-3FDFFFH	4088KB	L-511/512
1	0	0	1	1	0 to 63	000000H-3FBFFFH	4080KB	L-255/256
1	0	1	0	×	0 to 63	000000H-3F7FFFH	4064KB	L-127/128
1	0	1	1	0	0 to 63	000000H-3F7FFFH	4064KB	L-127/128
1	1	0	0	1	0 to 63	001000H-3FFFFFH	4092KB	U-1023/1024
1	1	0	1	0	0 to 63	002000H-3FFFFFH	4088KB	U-511/512
1	1	0	1	1	0 to 63	004000H-3FFFFFH	4080KB	U-255/256
1	1	1	0	×	0 to 63	008000H-3FFFFFH	4064KB	U-127/128
1	1	1	1	0	0 to 63	008000H-3FFFFFH	4064KB	U-127/128

6. STATUS REGISTER

S23	S22	S21	S20	S19	S18	S17	S16
Reserved	DRV1	DRV0	HPF	Reserved	Reserved	Reserved	Reserved

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, and BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, only if the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, power supply lock-down or one time programmable protection.

SRP1	SRP0	Status Register	Description
0	×	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Power Supply Lock-Down(1) (2)	Status Register is protected and can not be written to again until the next Power-Down, Power-Up cycle.
1	1	One Time Program(2)	Status Register is permanently protected and can not be written to.

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.

2. This feature is available on special order. Please contact GigaDevice for details.

QE bit.

The Quad Enable (QE) bit is a non-volatile bit in the Status Register that allows Quad operation. The default value of QE bit is 1 and it cannot be changed, so that the Quad IO2 and IO3 pins are enabled all the time.

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LB3, LB2, LB1 bits.

The LB3, LB2, LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB3-LB1 are 0, the security registers are unlocked. The LB3-LB1 bits can be set to 1 individually using the Write Register instruction. The LB3-LB1 bits are One Time Programmable, once its set to 1, the Security Registers will become read-only permanently.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

SUS1, SUS2 bits.

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS1 to 1,and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) command as well as a power-down, power-up cycle.

HPF bit.

The High Performance Flag (HPF) bit indicates the status of High Performance Mode (HPM). When HPF bit sets to 1, it means the device is in High Performance Mode, when HPF bit sets 0 (default), it means the device is not in High Performance Mode.

DRV1, DRV0 bits

The DRV1&DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
00	100%
01	75% (default)
10	50%
11	25%

7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the commands of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then CS# must be driven high to return to deselected status.

For the commands of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That means CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if CS# is driven high at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

<center>Table2. Commands (Standard/Dual/Quad SPI)</center>

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Volatile SR Write Enable	50H						
Read Status Register-1	05H	(S7-S0)					(continuous)
Read Status Register-2	35H	(S15-S8)					(continuous)
Read Status Register-3	15H	(S23-S16)					(continuous)
Write Status Register-1	01H	S7-S0					
Write Status Register-2	31H	S15-S8					
Write Status Register-3	11H	S23-S16					
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	D7-D0 [1]	(continuous)
Dual I/O Fast Read	BBH	A23-A8 [2]	A7-A0 M7-M0 [2]	(D7-D0) [1]	(Next byte)	(Next byte)	(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) [3]	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0 [4]	dummy [5]	(D7-D0) [3]	(Next byte)	(Next byte)	(continuous)
Quad I/O Word Fast Read [7]	E7H	A23-A0 M7-M0 [4]	dummy [6]	(D7-D0) [3]	(Next byte)	(Next byte)	(continuous)
Page Program	02H	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	D7-D0 [3]	Next byte	continuous
Fast Page Program	F2H	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase (32K)	52H	A23-A16	A15-A8	A7-A0			
Block Erase (64K)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Enable Reset	66H						
Reset	99H						

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Set Burst with Wrap	77H	dummy [9] W7-W0					
Program/Erase Suspend	75H						
Program/Erase Resume	7AH						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Deep Power-Down	B9H						
Manufacturer/ Device ID	90H	00H	00H	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Manufacturer/ Device ID by Dual I/O	92H	A23-A8	A7-A0, M7-M0	(MID7-MID0) (DID7-DID0)			(continuous)
Manufacturer/ Device ID by Quad I/O	94H	A23-A0, M7-M0	dummy [10] (MID7- MID0) (DID7-DID0)				(continuous)
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
High Performance Mode	A3H	dummy	dummy	dummy			
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Erase Security Registers [8]	44H	A23-A16	A15-A8	A7-A0			
Program Security Registers [8]	42H	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	continuous
Read Security Registers [8]	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)

NOTE:

(1) Dual Output data

IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

(2) Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8   A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9   A7, A5, A3, A1, M7, M5, M3, M1

(3) Quad Output Data

IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3, …..)

(4) Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

(5) Fast Read Quad I/O Data

IO0 = (x, x, x, x, D4, D0,…)
IO1 = (x, x, x, x, D5, D1,…)
IO2 = (x, x, x, x, D6, D2,…)
IO3 = (x, x, x, x, D7, D3,…)

(6) Fast Word Read Quad I/O Data

IO0 = (x, x, D4, D0,…)
IO1 = (x, x, D5, D1,…)
IO2 = (x, x, D6, D2,…)
IO3 = (x, x, D7, D3,…)

(7) Fast Word Read Quad I/O Data: the lowest address bit must be 0.

(8) Security Registers Address:

Security Register1: A23-A16=00H, A15-A10=000100b, A9-A0=Byte Address;
Security Register2: A23-A16=00H, A15-A10=001000b, A9-A0=Byte Address;
Security Register3: A23-A16=00H, A15-A10=001100b, A9-A0=Byte Address.

(9) Dummy bits and Wrap Bits

IO0 = (x, x, x, x, x, x, W4, x)
IO1 = (x, x, x, x, x, x, W5, x)
IO2 = (x, x, x, x, x, x, W6, x)
IO3 = (x, x, x, x, x, x, x, x)

(10) Address, Continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID

IO0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0, …)
IO1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1, …)
IO2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2, …)
IO3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3, …)

## Table Of ID Definitions:

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Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	C8	40	16
90H/92H/94H	C8		15
ABH			15

7.1. Write Enable (WREN)(06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR) and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: CS# goes low → sending the Write Enable command → CS# goes high.

Figure 1. Write Enable Sequence Diagram
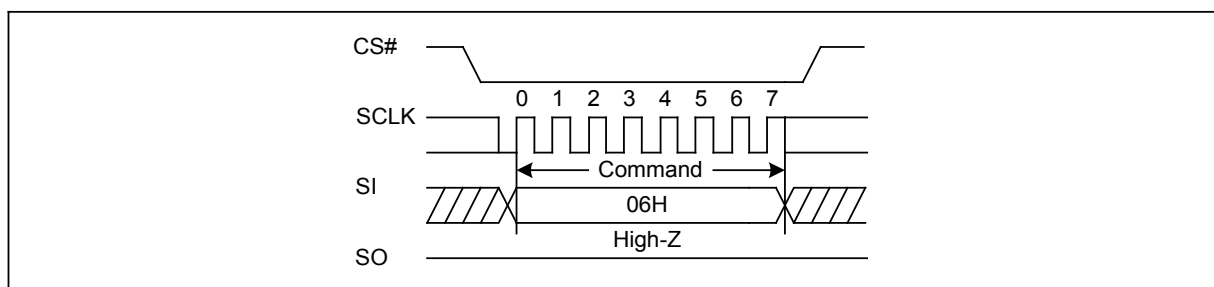
7.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase/Program Security Registers and Reset commands.

Figure 2. Write Disable Sequence Diagram
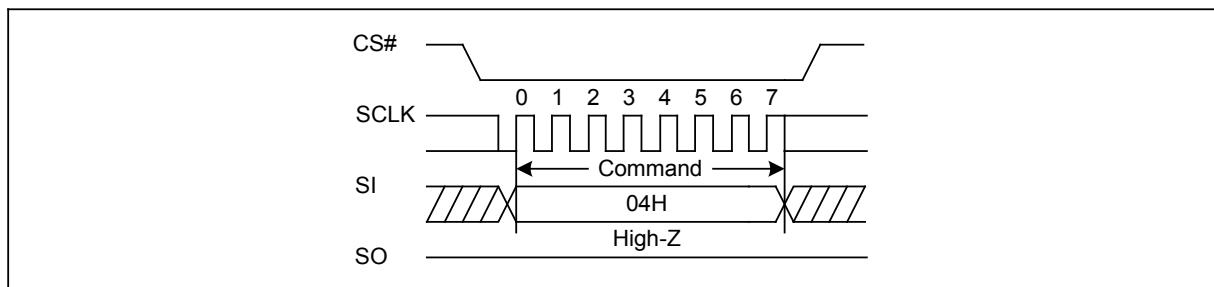
7.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command, and any other commands cannot be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 3. Write Enable for Volatile Status Register Sequence Diagram
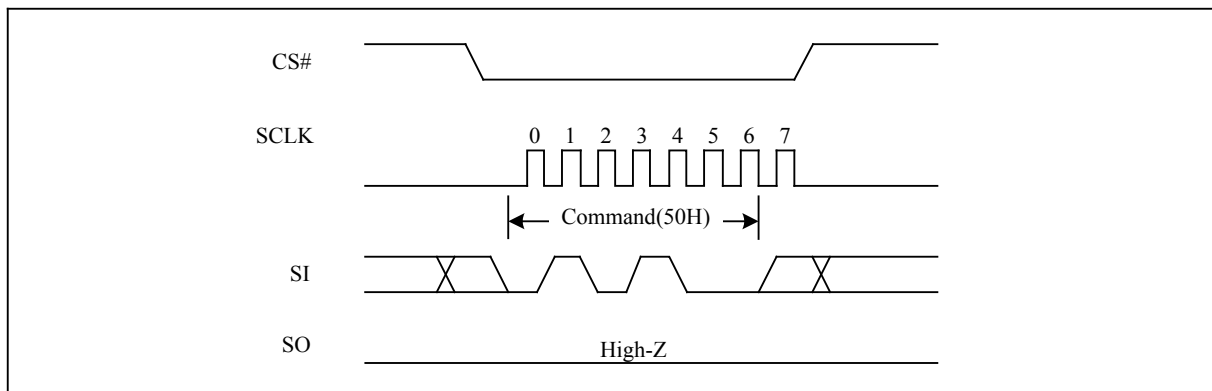
7.4. Read Status Register (RDSR) (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H" / "35H" / "15H", the SO will output Status Register bits S7~S0 / S15-S8 / S16-S23.

Figure 4. Read Status Register Sequence Diagram
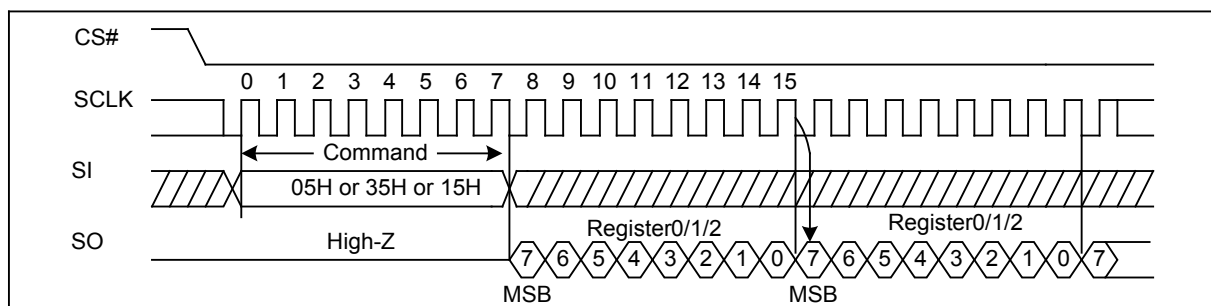
## 7.5. Write Status Register (WRSR) (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S23, S20, S19, S18, S17, S16, S15, S10, S1 and S0 of the Status Register. CS# must be driven high after the eighth of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only.
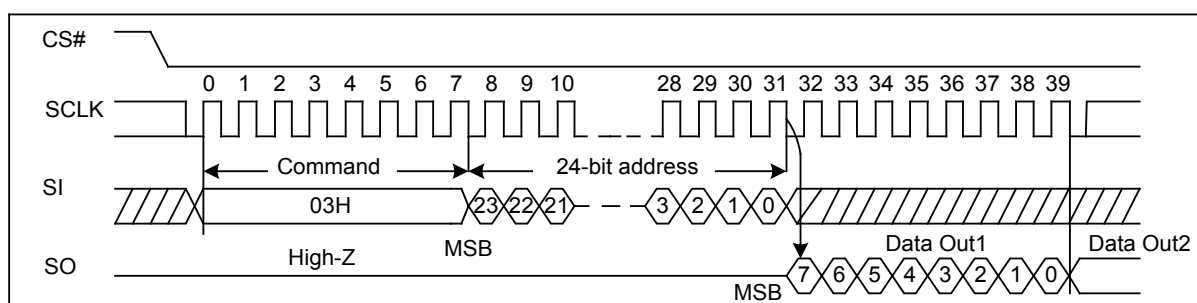
Figure 5. Write Status Register Sequence Diagram
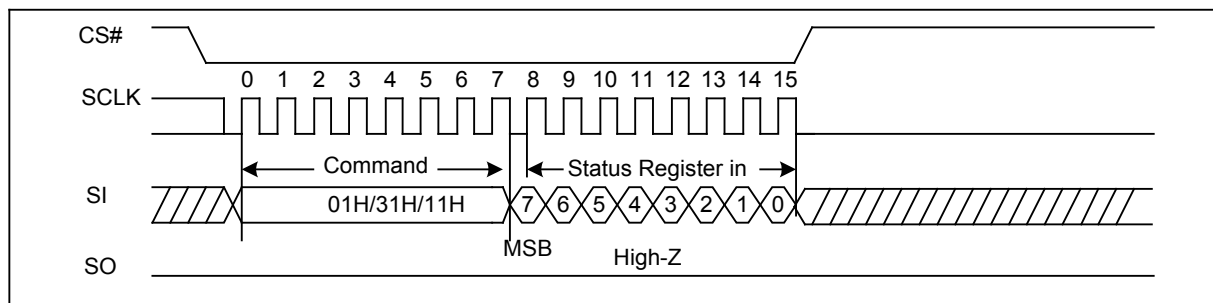
7.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 6. Read Data Bytes Sequence Diagram

7.7. Read Data Bytes at Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 7. Read Data Bytes at Higher Speed Sequence Diagram
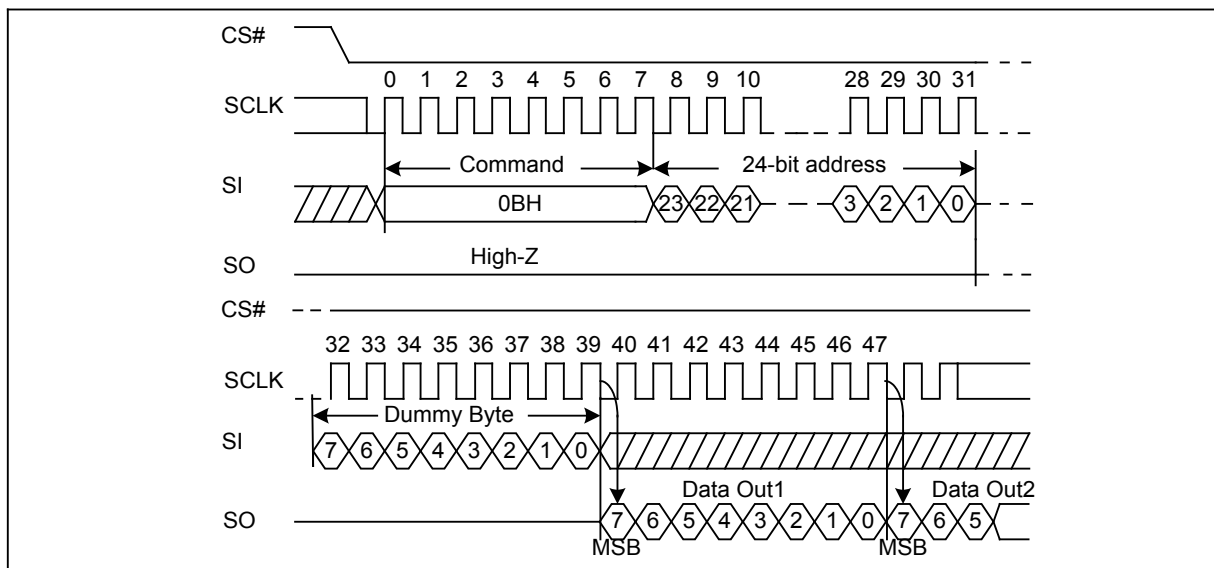
7.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.
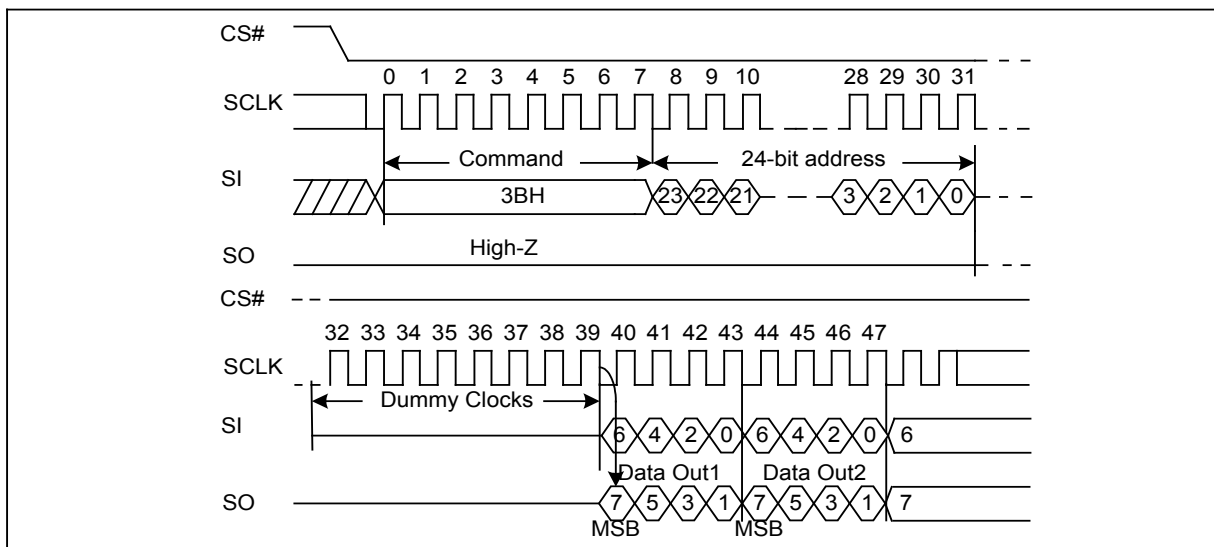
Figure 8. Dual Output Fast Read Sequence Diagram

7.9. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 9. Quad Output Fast Read Sequence Diagram
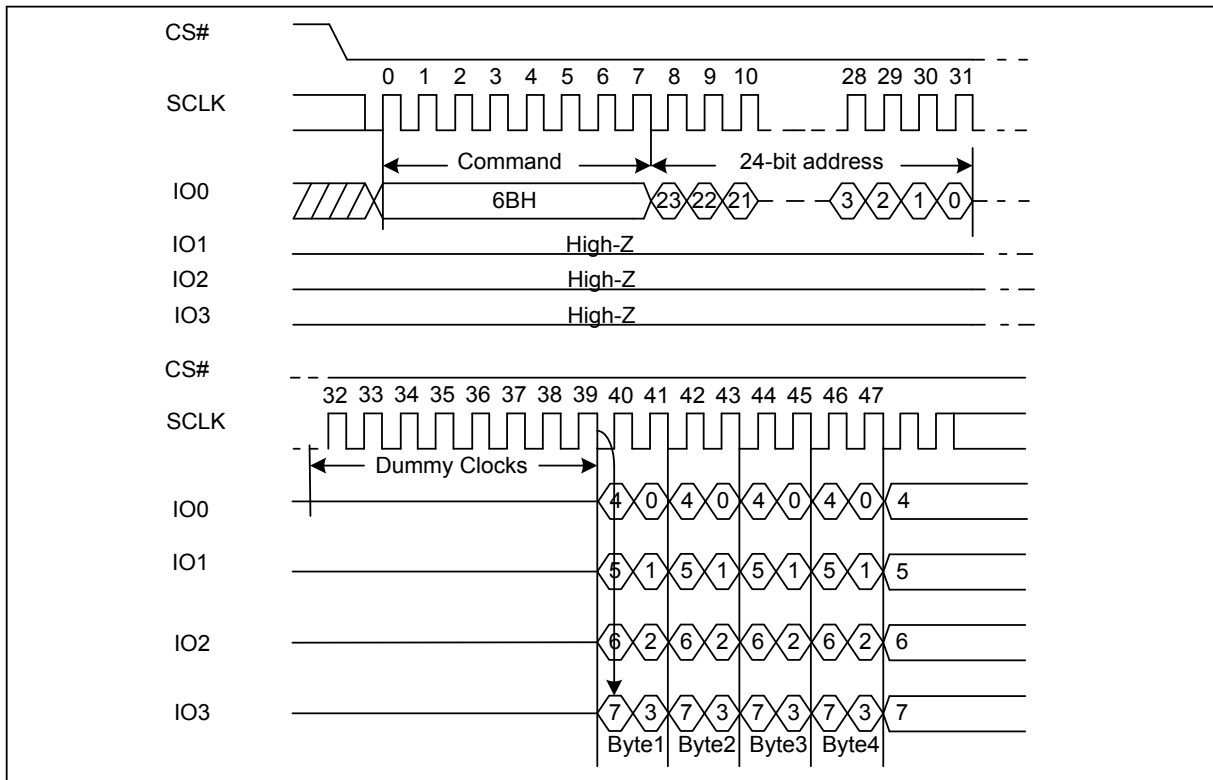
7.10. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-4) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure11. If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

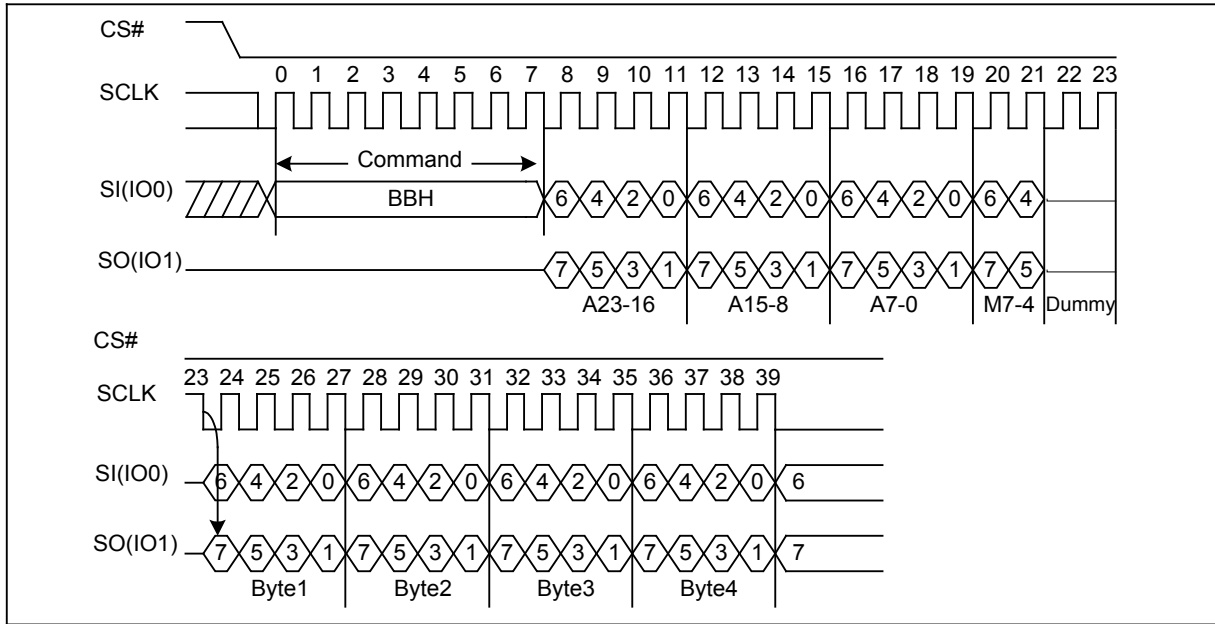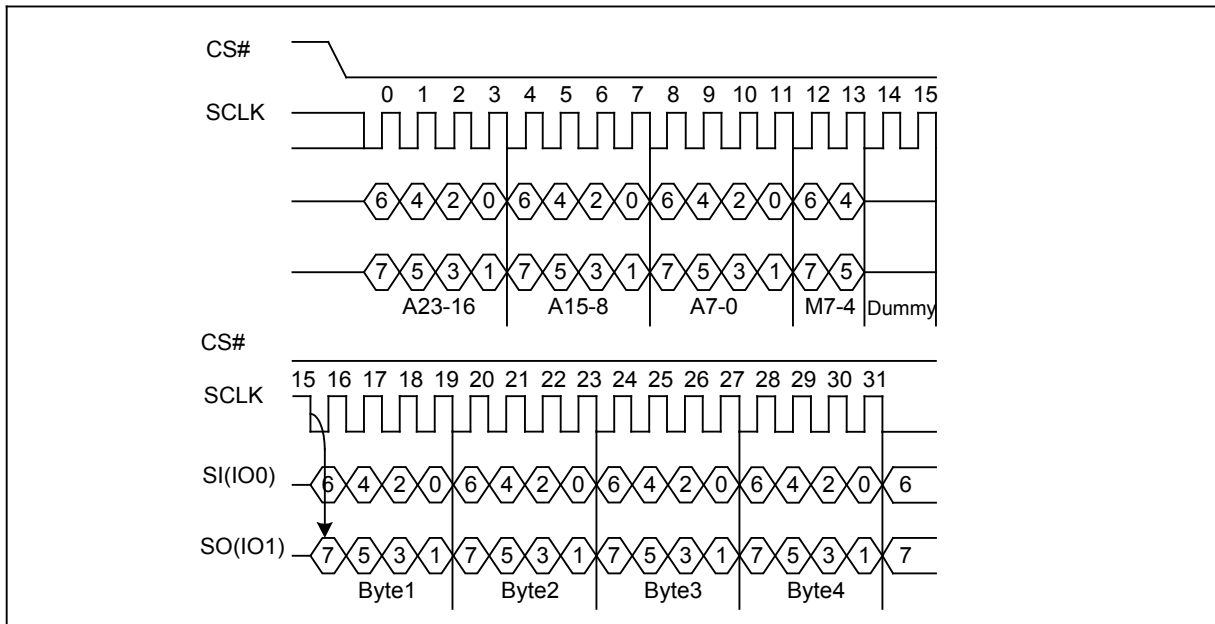Figure 10. Dual I/O Fast Read Sequence Diagram (M5-4 ≠ (1, 0))

Figure 11. Dual I/O Fast Read Sequence Diagram (M5-4 = (1, 0))

7.11. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO2, IO3, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure12. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure13. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

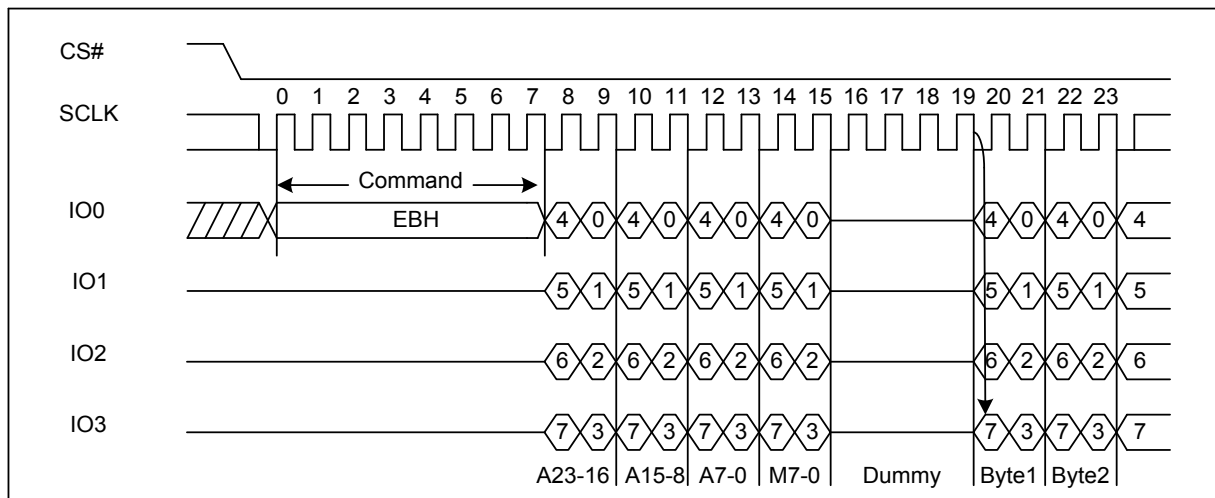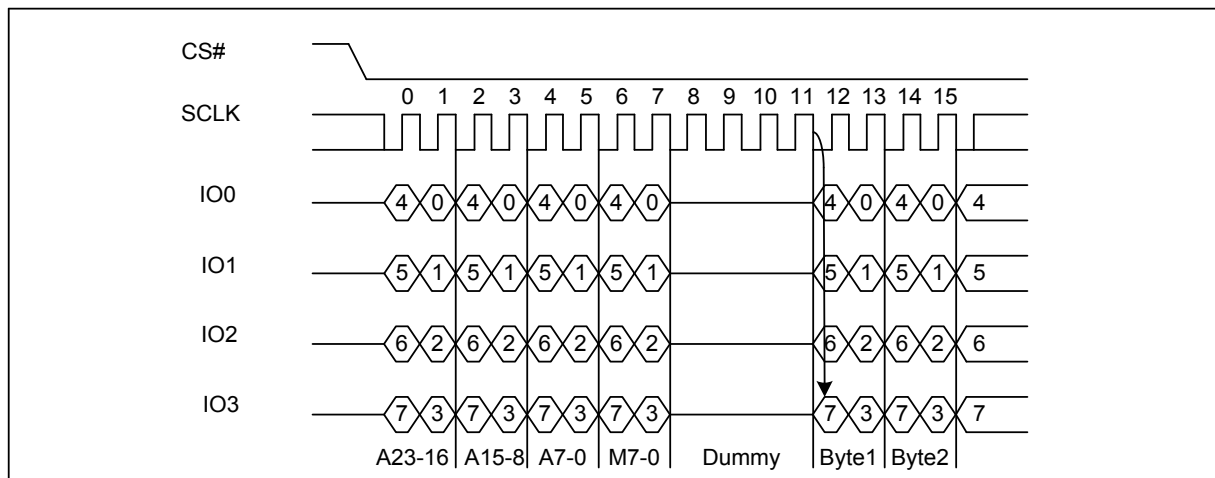Figure 12. Quad I/O Fast Read Sequence Diagram (M5-4 ≠ (1, 0))

Figure 13. Quad I/O Fast Read Sequence Diagram (M5-4 = (1, 0))

Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.12. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure15. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

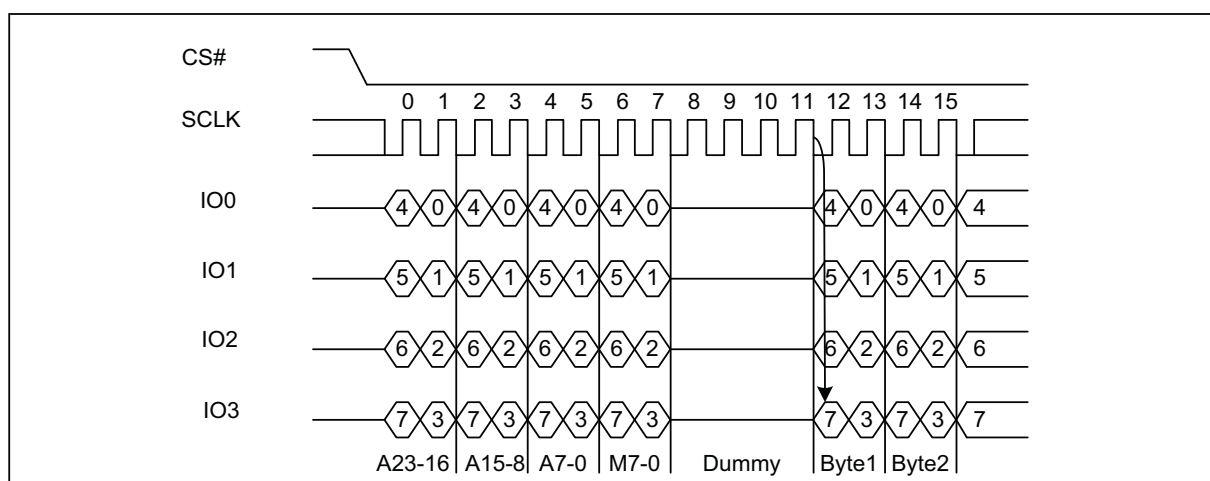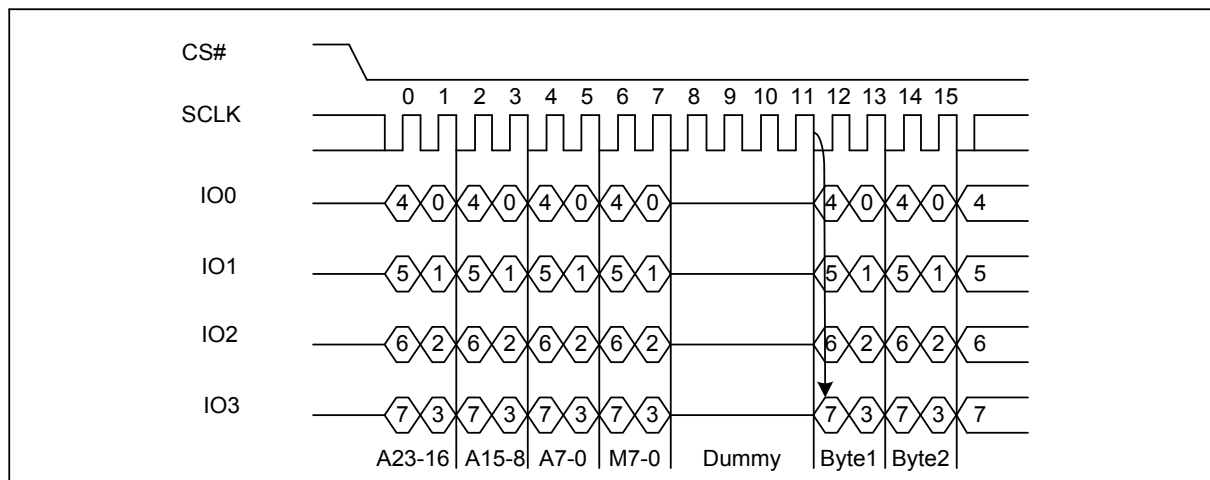Figure 14. Quad I/O Word Fast Read Sequence Diagram (M5-4≠ (1, 0))

Figure 15. Quad I/O Word Fast Read Sequence Diagram (M5-4= (1, 0))

Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to E7H. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following E7H commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

7.13. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: CS# goes low → Send Set Burst with Wrap command → Send 24 dummy bits → Send 8 bits "Wrap bits" → CS# goes high.

W6, W5	W4=0		W4=1 (default)	
	Wrap Around	**Wrap Length**	**Wrap Around**	**Wrap Length**
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

Figure 16. Set Burst with Wrap Sequence Diagram
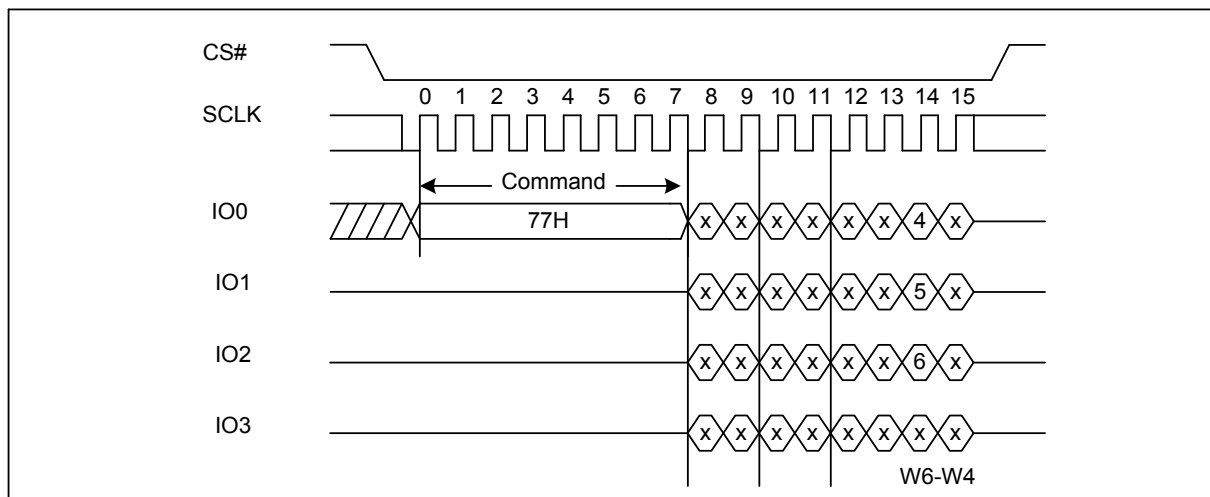
7.14. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.
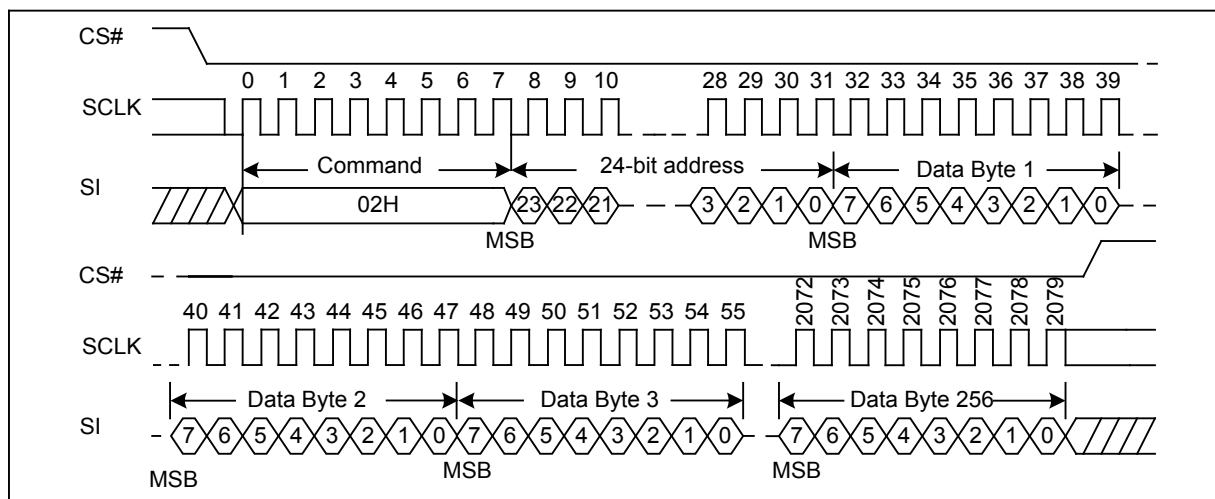
The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in Figure17. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 17. Page Program Sequence Diagram

7.15. Quad Page Program (32H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure18. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) is not executed.

Figure 18. Quad Page Program Sequence Diagram
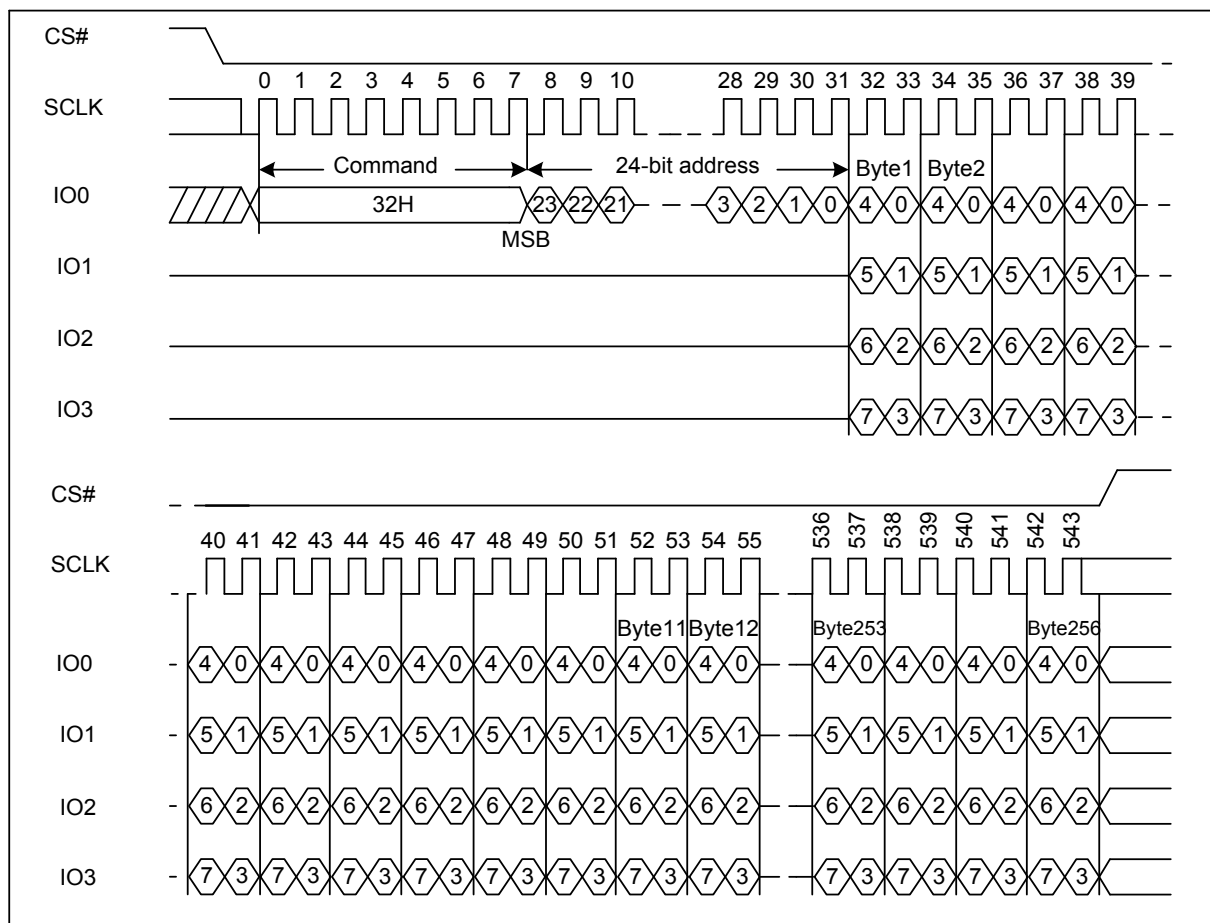
7.16. Fast Page Program (FPP) (F2H)

The Fast Page Program (FPP) command is used to program the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Fast Page Program (FPP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence.

The Page Program command sequence: CS# goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high.

The command sequence is shown in Figure19. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Fast Page Program (FPP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when

it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Fast Page Program (FPP) command is not executed when it is applied to a page protected by the Block Protect (BP4, BP3, BP2, BP1, BP0).

Figure 19. Fast Page Program Sequence Diagram
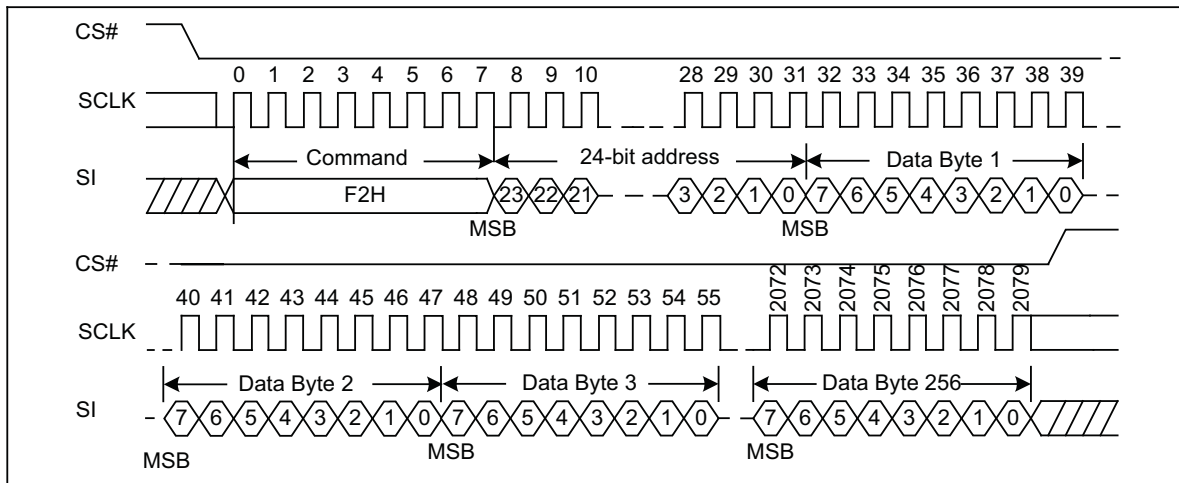
7.17. Sector Erase (SE) (20H)

The Sector Erase (SE) command is used to erase all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low → sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure20. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bit (see Table1&1a) is not executed.
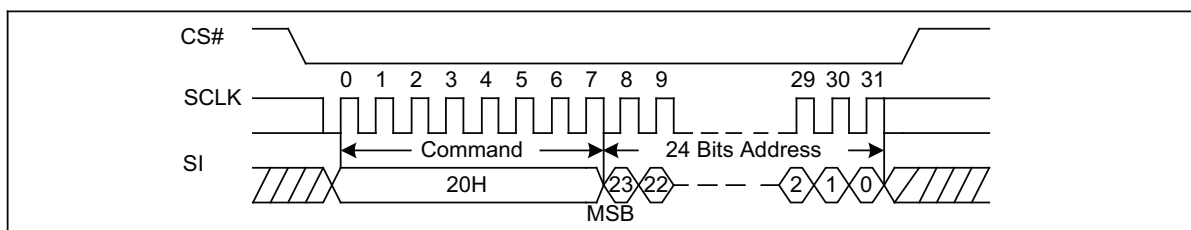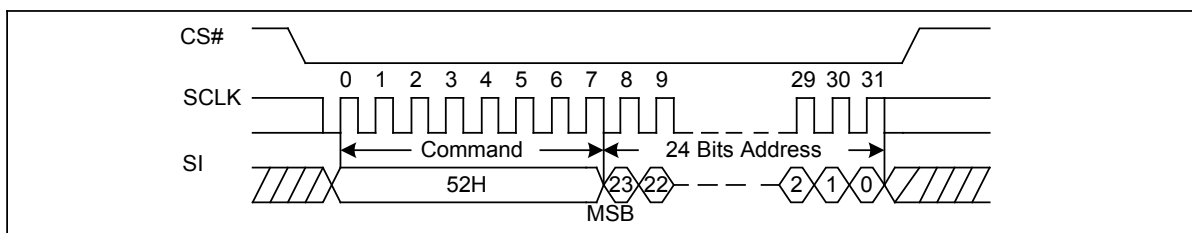
Figure 20. Sector Erase Sequence Diagram

7.18. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is used to erase all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low → sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure21. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits (see Table1&1a) is not executed.

Figure 21. 32KB Block Erase Sequence Diagram

7.19. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is used to erase all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low → sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in Figure22. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits (see Table1&1a) is not executed.
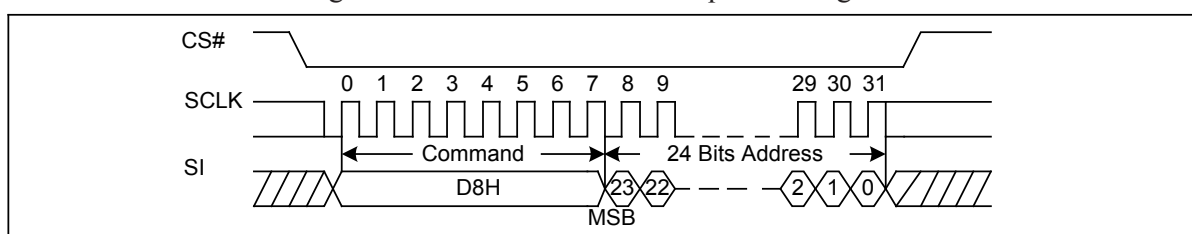
Figure 22. 64KB Block Erase Sequence Diagram

7.20. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is used to erase all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low → sending Chip Erase command → CS# goes high. The command sequence is shown in Figure23. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Figure 23. Chip Erase Sequence Diagram
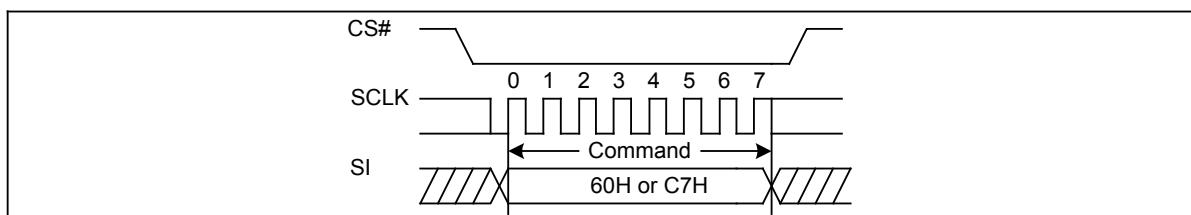
7.21. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low → sending Deep Power-Down command → CS# goes high. The command sequence is shown in Figure24. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 24. Deep Power-Down Sequence Diagram
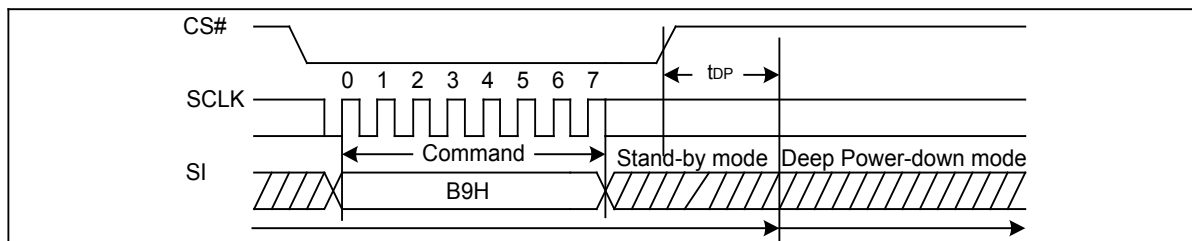
7.22. Release from Deep Power-Down or High Performance Mode and Read Device ID (RDI) (ABH)

The Release from Power-Down or High Performance Mode / Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or High Performance Mode or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state or High Performance Mode, the command is issued by driving the CS# pin low, shifting the instruction code "ABH" and driving CS# high as shown in Figure25. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure26. The Device ID value for the GD25B32C is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure26, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 25. Release Power-Down Sequence or High Performance Mode Sequence Diagram
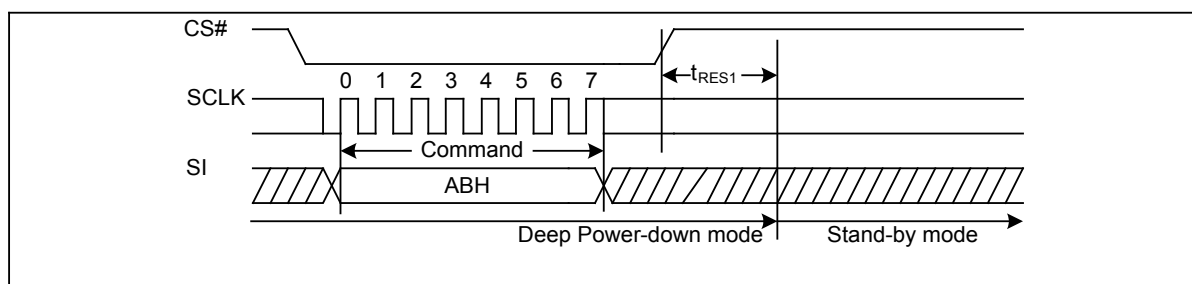
Figure 26. Release Power-Down/Read Device ID Sequence Diagram
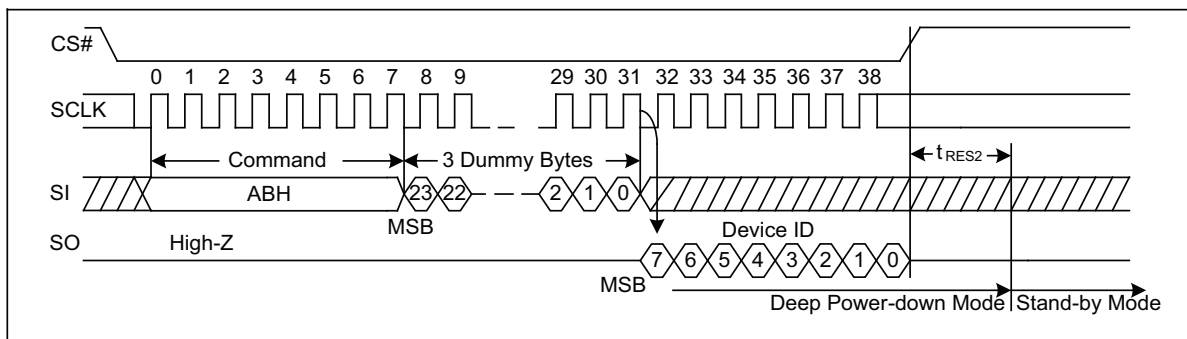
7.23. Read Manufacture ID/Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure27. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 27. Read Manufacture ID/Device ID Sequence Diagram
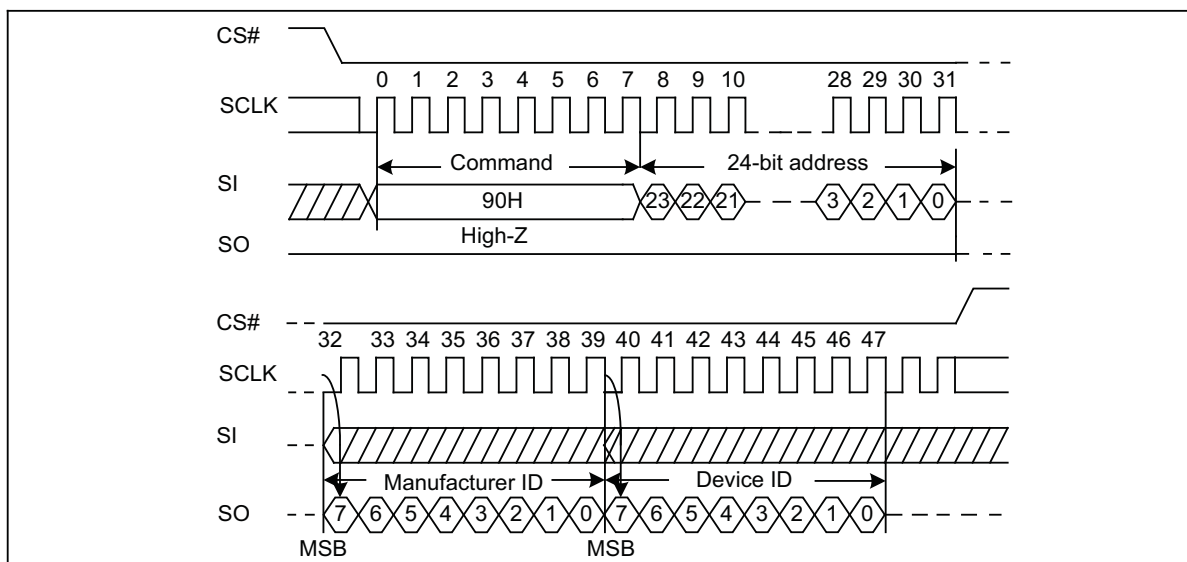
7.24. Dual I/O Read Manufacture ID/Device ID (92H)

The Dual I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code "92H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure28. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 28. Read Manufacture ID/Device ID Dual I/O Sequence Diagram
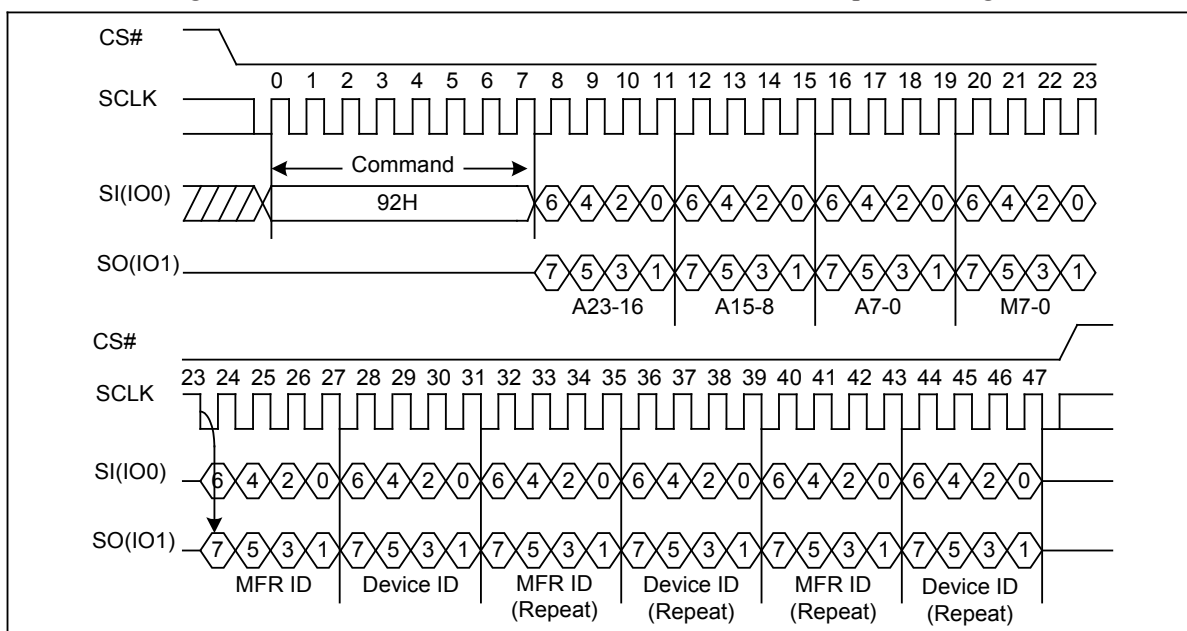
7.25. Quad I/O Read Manufacture ID/Device ID (94H)

The Quad I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code "94H" followed by a 24-bit address (A23-A0) of 000000H , and 4 dummy clocks. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure29. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 29. Read Manufacture ID/Device ID Quad I/O Sequence Diagram
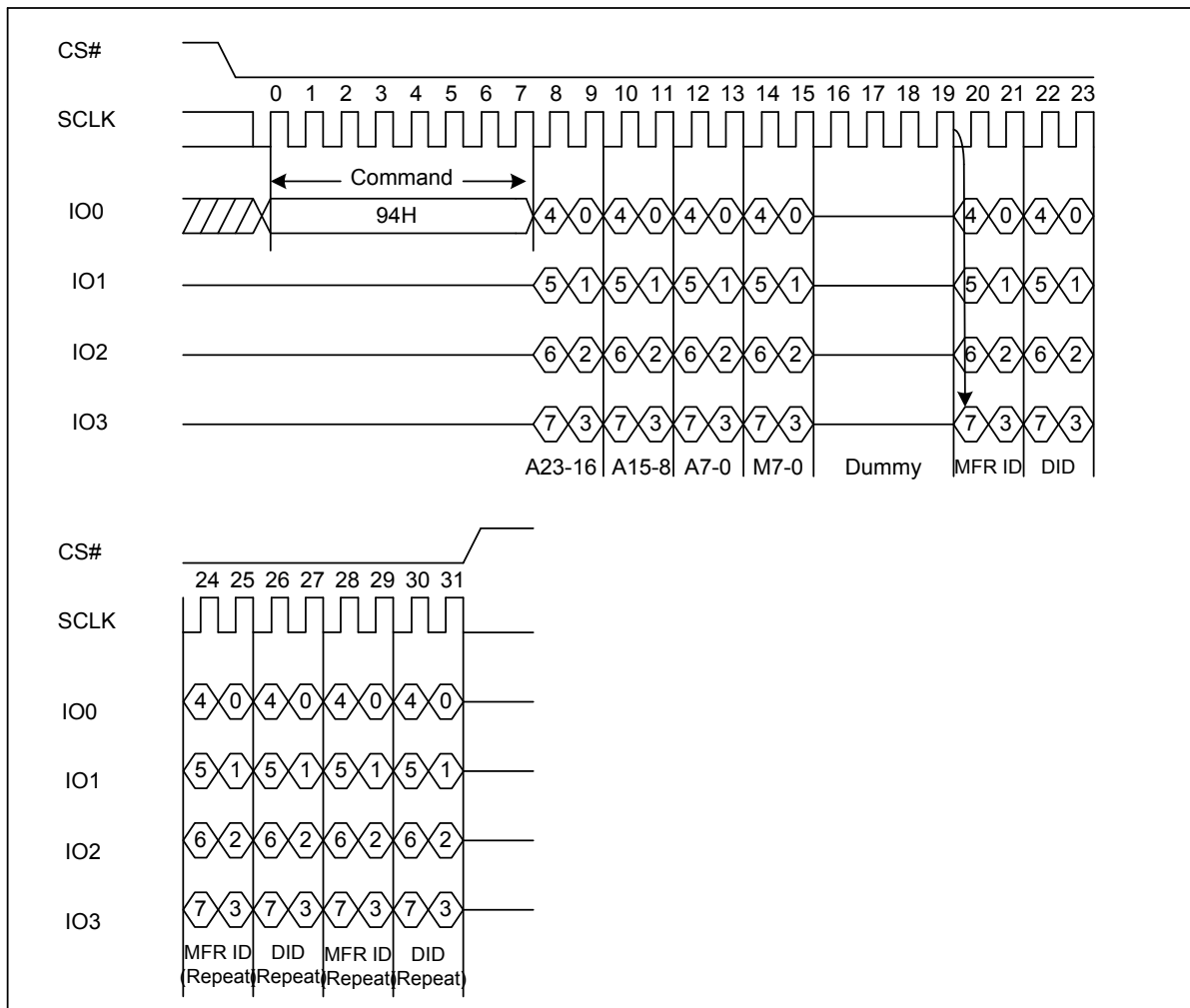
7.26. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. The Read Identification (RDID) command while an Erase or Program cycle is in progress is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure30. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 30. Read Identification ID Sequence Diagram
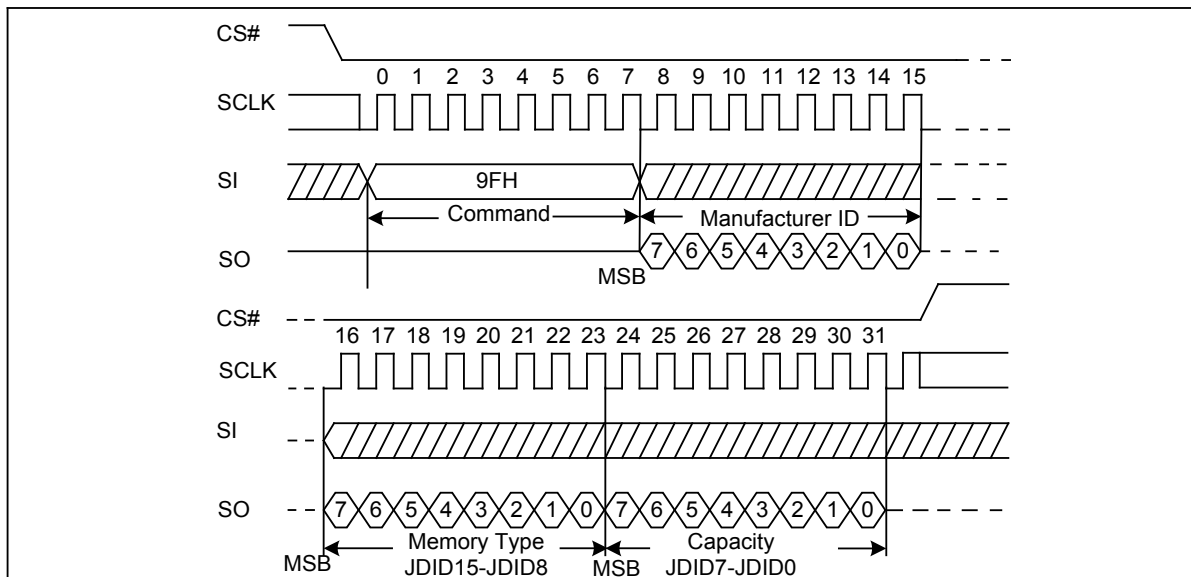
7.27. High Performance Mode (HPM) (A3H)

The High Performance Mode (HPM) command must be executed prior to Dual or Quad I/O commands when operating at high frequencies (see fR and fC2 in AC Electrical Characteristics). This command allows pre-charging of internal charge pumps so the voltages required for accessing the flash memory array are readily available. The command sequence: CS# goes low → Sending A3H command → Sending 3-dummy byte → CS# goes high. See Figure31. After the HPM command is executed, the device will maintain a slightly higher standby current (Icc8) than standard SPI operation. The Release from Power-Down or HPM command (ABH) can be used to return to standard SPI standby current (Icc1). In addition, Power-Down command (B9H) will also release the device from HPM mode back to standard SPI standby state.

Figure 31. High Performance Mode Sequence Diagram
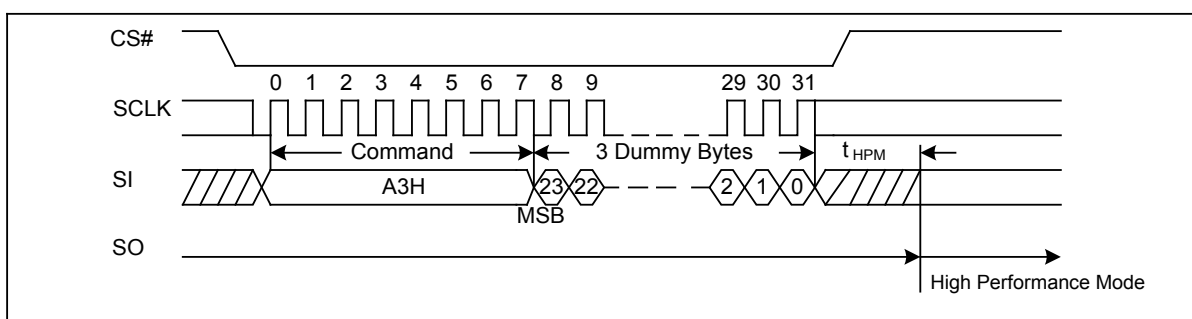
7.28. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command → 3-Byte Address (000000H) → Dummy Byte → 128bit Unique ID Out → CS# goes high.

Figure 32. Read Unique ID Sequence Diagram
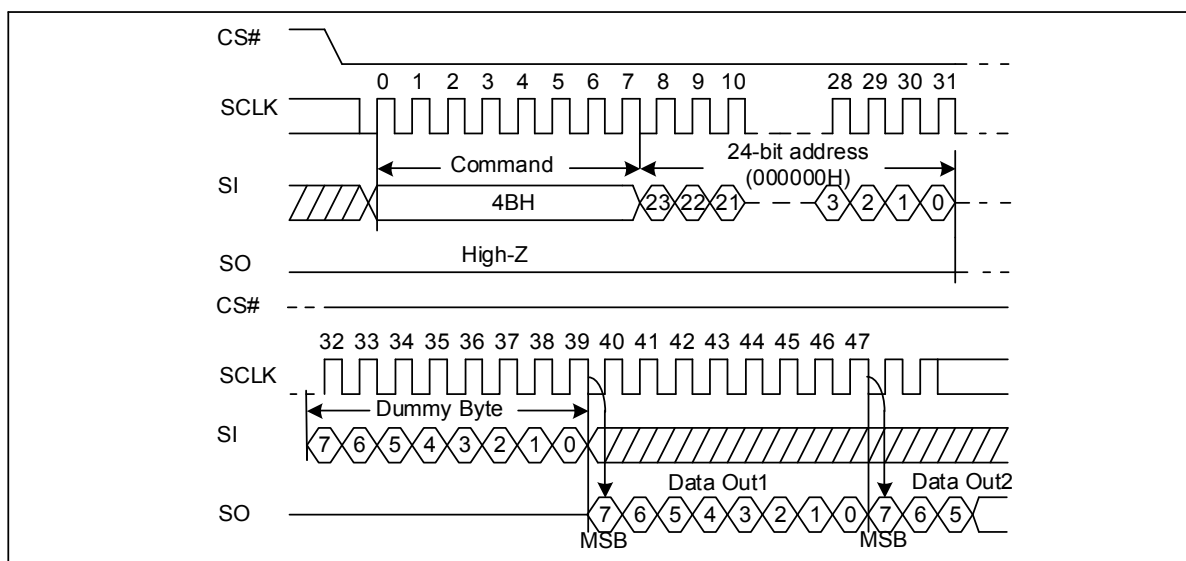
7.29. Program/Erase Suspend (PES) (75H)

The Program/Erase Suspend command "75H", allows the system to interrupt a page program or sector/ block erase operation and then read data from any other sector or block. The Write Status Register command (01H/31H/11H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 52H, D8H, C7H, 60H) and Page Program command (02H / 32H) are not allowed during Program/Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of "tsus" (See AC Characteristics) is required to suspend the program/erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS2/SUS1 bit in the Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS2/SUS1 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tsus" and the SUS2/SUS1 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is show below.

Figure 33. Program/Erase Suspend Sequence Diagram
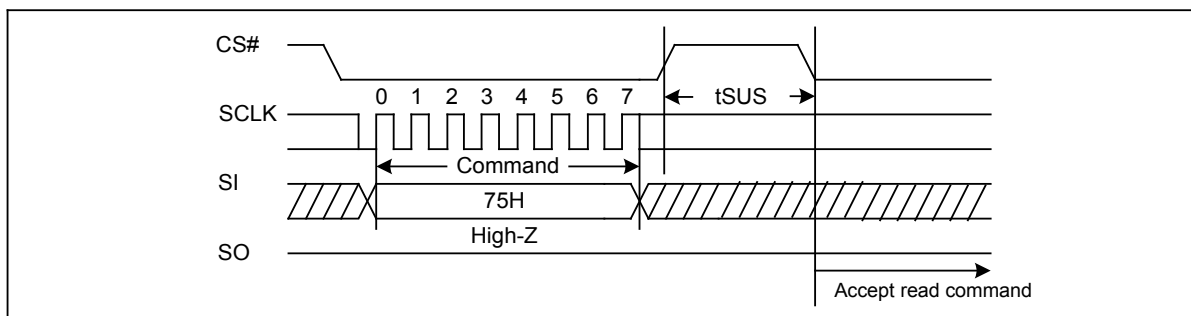
7.30. Program/Erase Resume (PER) (7AH)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase command will be accepted by the device only if the SUS2/SUS1 bit equal to 1 and the WIP bit equal to 0. After issued the SUS2/SUS1 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is show in Figure34.

Figure 34. Program/Erase Resume Sequence Diagram
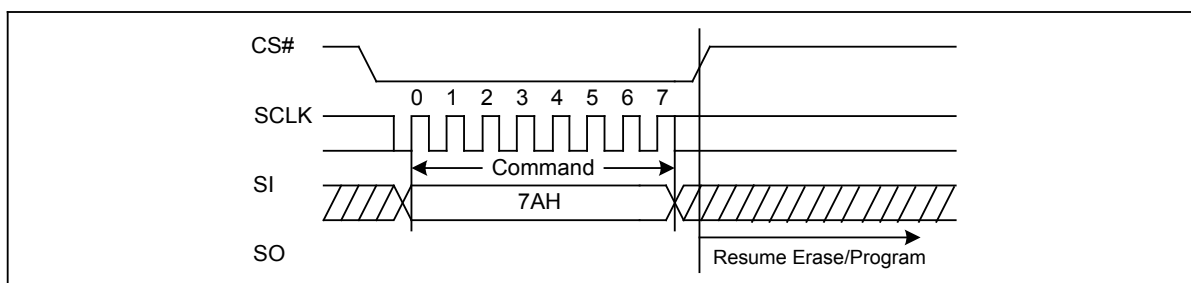
7.31. Erase Security Registers (44H)

The GD25B32C provides three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → sending Erase Security Registers command → CS# goes high. The command sequence is shown in Figure35. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB3-1) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Register #1	00H	0 0 0 1	0 0	Don't care
Security Register #2	00H	0 0 1 0	0 0	Don't care
Security Register #3	00H	0 0 1 1	0 0	Don't care

Figure 35. Erase Security Registers command Sequence Diagram
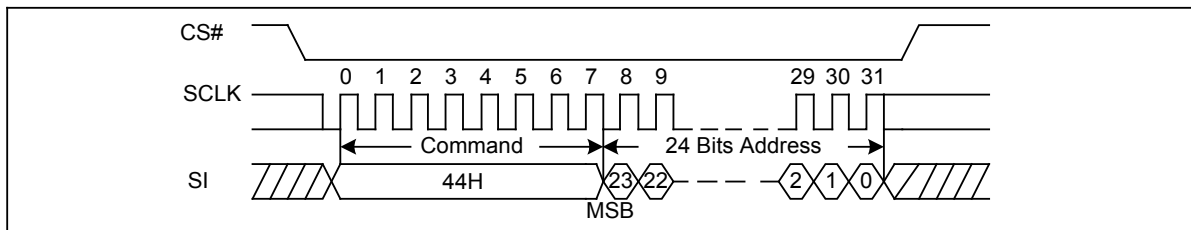
7.32. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1024 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB3-1) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 36. Program Security Registers command Sequence Diagram

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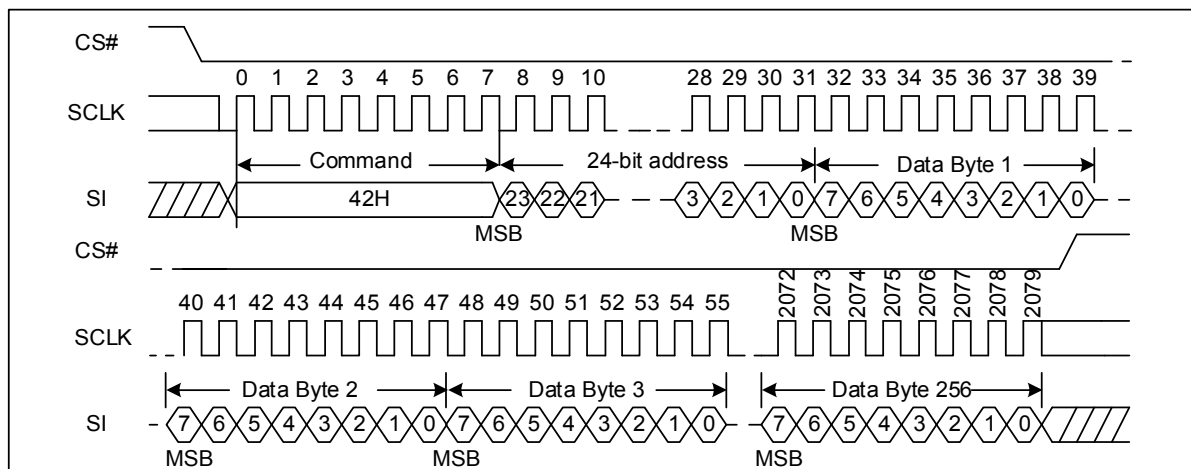
7.33. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command I is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 37. Read Security Registers command Sequence Diagram
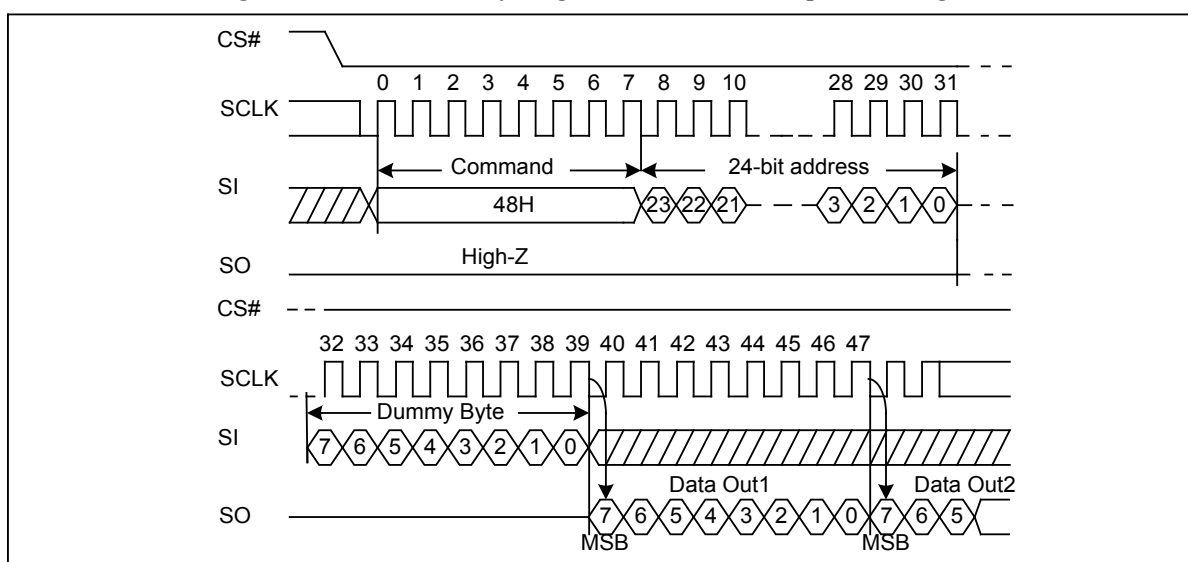
7.34. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST / tRST_E to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 38. Enable Reset and Reset command Sequence Diagram
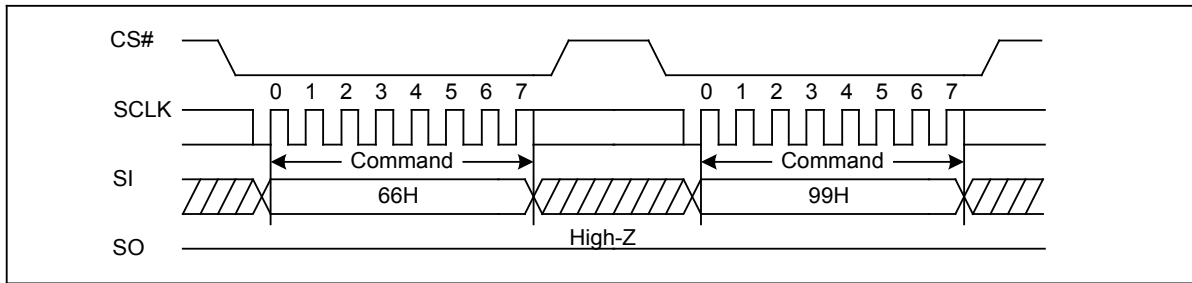
7.35. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Figure 39. Read Serial Flash Discoverable Parameter command Sequence Diagram
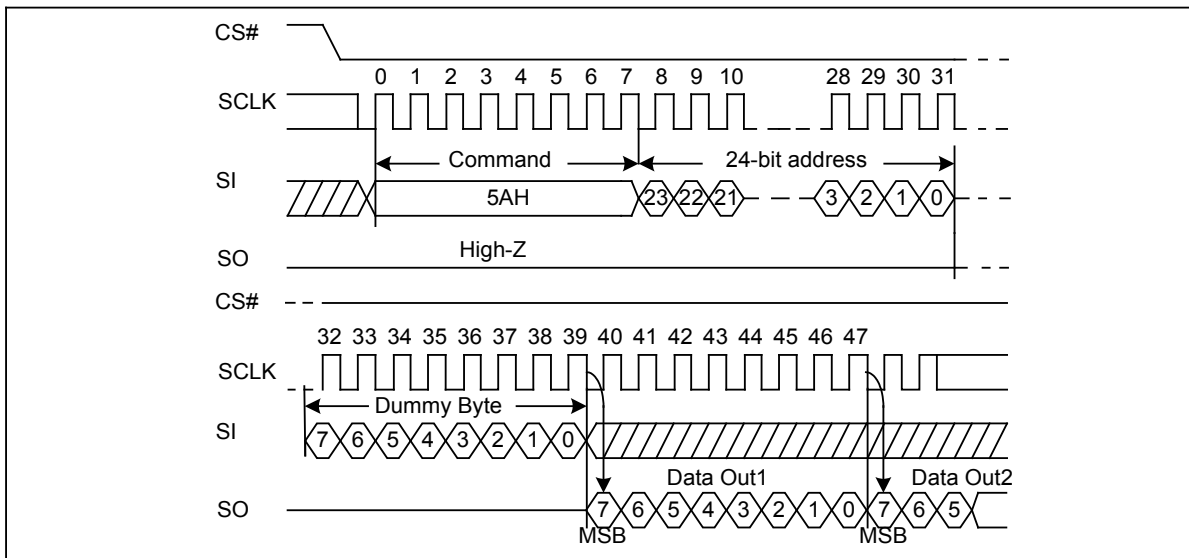
Table3. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDF Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDF Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0×FFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0×00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0×01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter Table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	Fist address of JEDEC Flash Parameter Table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0×FFH and can never be changed	0FH	31:24	FFH	FFH
ID Number (GigaDevice Manufacturer ID)	It is indicates GigaDevice manufacturer ID	10H	07:00	C8H	C8H
Parameter Table Minor Revision Number	Start from 0×00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0×01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter Table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	Fist address of GigaDevice Flash Parameter Table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0×FFH and can never be changed	17H	31:24	FFH	FFH

Table4. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	01FFFFFFH	
(1-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1-1-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1-2-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3EH	20:16	00010b	42H
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support; 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support; 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0×FFH	0×FFH
Unused		45H:44H	15:00	0×FFH	0×FFH
(2-2-2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0×FFH	0×FFH
(4-4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0×00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0×00b: this sector type don't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0×00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0×00b: this sector type don't exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

Table5. Parameter Table (1): GigaDevice Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	2700H	2700H
HW Reset# pin	0=not support; 1=support	65H:64H	00	0b	F99CH
HW Hold# pin	0=not support; 1=support		01	0b	
Deep Power Down Mode	0=not support; 1=support		02	1b	
SW Reset	0=not support; 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H) before Reset cmd.		11:04	1001 1001b (99H)	
Program Suspend/Resume	0=not support; 1=support		12	1b	
Erase Suspend/Resume	0=not support; 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support; 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H: support 8B wrap-around read 16H: 8B & 16B 32H: 8B & 16B & 32B 64H: 8B & 16B & 32B & 64B	67H	31:24	64H	64H
Individual block lock	0=not support; 1=support	6BH:68H	00	0b	EBFCH
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile; 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect; 1=unprotect		10	0b	
Secured OTP	0=not support; 1=support		11	1b	
Read Lock	0=not support; 1=support		12	0b	
Permanent Lock	0=not support; 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

8. ELECTRICAL CHARACTERISTICS

8.1. POWER-ON TIMING
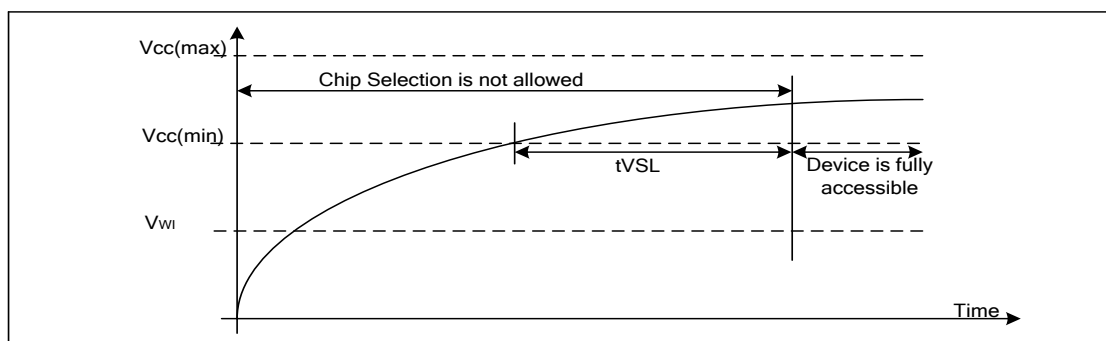
Table6. Power-Up Timing And Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# Low	1.8		ms
VWI	Write Inhibit Voltage VCC(min)	1.5	2.5	V

8.2. INITIAL DELIVERY STATE

 The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register bits are set to 0, except DRV0 bit (S21) and QE bit (S9) are set to 1.

8.3. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	°C
	-40 to 105	
	-40 to 125	
Storage Temperature	-65 to 150	°C
Applied Input/Output Voltage	-0.6 to VCC+0.4	V
Transient Input/Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
VCC	-0.6 to 4.2	V

Figure 39. Maximum Negative/positive Overshoot Diagram
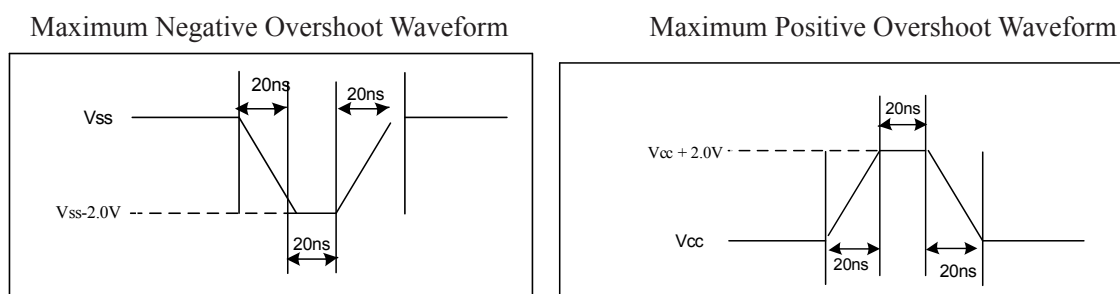
8.4. CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure 40. Input Test Waveform and Measurement Level Diagram

8.5. DC CHARACTERISTICS

(T= -40°C~85°C, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		1	5	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/0.9VCC at 120MHz, Q=Open(*1,*2,*4 I/O)		15	20	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC			25	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC			25	mA
I_{CC6}	Operating Current (SE)	CS#=VCC			25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC			25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC			25	mA
I_{CC9}	High Performance Current			0.6	1.2	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL}=100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH}=-100μA	VCC-0.2			V

Note:

1. Typical values given for TA=25°C.

2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T= -40°C~105°C, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		1	20	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		1	20	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		15	20	mA
		CLK=0.1VCC/0.9VCC at 60MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC			25	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC			25	mA
I_{CC6}	Operating Current (SE)	CS#=VCC			25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC			25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC			25	mA
I_{CC9}	High Performance Current			0.6	1.5	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL}=100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH}=-100μA	VCC-0.2			V

Note:
1. Typical values given for TA=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

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(T= -40°C~125°C, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS		1	25	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC, V_{IN}=VCC or VSS		1	25	μA
I_{CC3}	Operating Current (Read)	CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		15	20	mA
		CLK=0.1VCC/0.9VCC at 60MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
I_{CC4}	Operating Current (PP)	CS#=VCC			25	mA
I_{CC5}	Operating Current (WRSR)	CS#=VCC			25	mA
I_{CC6}	Operating Current (SE)	CS#=VCC			25	mA
I_{CC7}	Operating Current (BE)	CS#=VCC			25	mA
I_{CC8}	Operating Current (CE)	CS#=VCC			25	mA
I_{CC9}	High Performance Current			0.6	1.5	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL}=100μA			0.2	V
V_{OH}	Output High Voltage	I_{OH}=-100μA	VCC-0.2			V

Note:
1. Typical values given for TA=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

8.6. AC CHARACTERISTICS

(T= -40°C~85°C, VCC=2.7~3.6V, C$_L$=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f$_C$	Serial Clock Frequency For: Dual I/O (BBH), Quad I/O(EBH), Quad Output(6BH) (Dual I/O & Quad I/O Without High Performance Mode), on 3.0V-3.6V power supply			104	MHz
f$_{C1}$	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O (EBH), Quad Output(6BH) (Dual I/O & Quad I/O Without High Performance Mode), on 2.7V-3.0V power supply			80	MHz
f$_{C2}$	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O (EBH), Quad Output(6BH) (Dual I/O & Quad I/O With High Performance Mode), on 2.7V-3.6V power supply			120	MHz
f$_R$	Serial Clock Frequency For: Read (03H) Read ID (90H, 9FH and ABH), Read Status Register (05H and 35H)			80	MHz
t$_{CLH}$	Serial Clock High Time	4			ns
t$_{CLL}$	Serial Clock Low Time	4			ns
t$_{CLCH}$	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t$_{CHCL}$	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t$_{SLCH}$	CS# Active Setup Time	5			ns
t$_{CHSH}$	CS# Active Hold Time	5			ns
t$_{SHCH}$	CS# Not Active Setup Time	5			ns
t$_{CHSL}$	CS# Not Active Hold Time	5			ns
t$_{SHSL}$	CS# High Time (Read/Write)	20			ns
t$_{SHQZ}$	Output Disable Time			6	ns
t$_{CLQX}$	Output Hold Time	1.2			ns
t$_{DVCH}$	Data In Setup Time	2			ns
t$_{CHDX}$	Data In Hold Time	2			ns
t$_{CLQV}$	Clock Low To Output Valid			7	ns
t$_{DP}$	CS# High To Deep Power-Down Mode			20	μs
t$_{RES1}$	CS# High To Standby Mode Without Electronic Signature Read			20	μs
t$_{RES2}$	CS# High To Standby Mode With Electronic Signature Read			20	μs
t$_{SUS}$	CS# High To Next Command After Suspend			20	μs
t$_{RS}$	Latency Between Resume And Next Suspend	100			μs
t$_{RST}$	CS# High To Next Command After Reset(Except From Erase)			30	μs
t$_{RST\_E}$	CS# High To Next Command After Reset (From Erase)			12	ms
t$_W$	Write Status Register Cycle Time		5	30	ms
t$_{BP1}$	Byte Program Time (First Byte)		30	50	μs
t$_{BP2}$	Additional Byte Program Time (After First Byte)		2.5	12	μs
t$_{PP}$	Page Programming Time		0.6	2.4	ms
t$_{SE}$	Sector Erase Time (4K Bytes)		50	300	ms

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tBE1	Block Erase Time (32K Bytes)		0.15	1.6	s
tBE2	Block Erase Time (64K Bytes)		0.25	2.0	s
tCE	Chip Erase Time (GD25B32C)		15	30	s

Note:

1. Typical value tested at TA= 25°C.

2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T= -40°C~105°C, VCC=2.7~3.6V, C$_L$=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
f$_C$	Serial Clock Frequency For: Dual I/O (BBH), Quad I/O(EBH), Quad Output(6BH) (Dual I/O & Quad I/O Without High Performance Mode), on 3.0V-3.6V power supply			80	MHz
f$_{C1}$	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O (EBH), Quad Output(6BH) (Dual I/O & Quad I/O Without High Performance Mode), on 2.7V-3.0V power supply			70	MHz
f$_{C2}$	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O (EBH), Quad Output(6BH) (Dual I/O & Quad I/O With High Performance Mode), on 2.7V-3.6V power supply			80	MHz
f$_R$	Serial Clock Frequency For: Read (03H) Read ID (90H, 9FH and ABH), Read Status Register (05H and 35H)			60	MHz
t$_{CLH}$	Serial Clock High Time	4			ns
t$_{CLL}$	Serial Clock Low Time	4			ns
t$_{CLCH}$	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t$_{CHCL}$	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t$_{SLCH}$	CS# Active Setup Time	5			ns
t$_{CHSH}$	CS# Active Hold Time	5			ns
t$_{SHCH}$	CS# Not Active Setup Time	5			ns
t$_{CHSL}$	CS# Not Active Hold Time	5			ns
t$_{SHSL}$	CS# High Time (Read/Write)	20			ns
t$_{SHQZ}$	Output Disable Time			6	ns
t$_{CLQX}$	Output Hold Time	0.7			ns
t$_{DVCH}$	Data In Setup Time	2			ns
t$_{CHDX}$	Data In Hold Time	2			ns
t$_{CLQV}$	Clock Low To Output Valid			7	ns
t$_{DP}$	CS# High To Deep Power-Down Mode			20	μs
t$_{RES1}$	CS# High To Standby Mode Without Electronic Signature Read			20	μs
t$_{RES2}$	CS# High To Standby Mode With Electronic Signature Read			20	μs
t$_{SUS}$	CS# High To Next Command After Suspend			20	μs
t$_{RS}$	Latency Between Resume And Next Suspend	100			μs
t$_{RST}$	CS# High To Next Command After Reset(Except From Erase)			30	μs
t$_{RST\_E}$	CS# High To Next Command After Reset (From Erase)			12	ms
t$_W$	Write Status Register Cycle Time		5	30	ms
t$_{BP1}$	Byte Program Time (First Byte)		30	60	μs
t$_{BP2}$	Additional Byte Program Time (After First Byte)		2.5	15	μs
t$_{PP}$	Page Programming Time		0.6	4	ms
t$_{SE}$	Sector Erase Time (4K Bytes)		50	400	ms

Symbol	Parameter	Min.	Typ.	Max.	Unit.
t_{BE1}	Block Erase Time (32K Bytes)		0.2	1.6	s
t_{BE2}	Block Erase Time (64K Bytes)		0.3	3.0	s
t_{CE}	Chip Erase Time (GD25B32C)		15	70	s

Note:

1. Typical value tested at TA = 25°C.

2. Value guaranteed by design and/or characterization, not 100% tested in production.

(T= -40°C~125°C, VCC=2.7~3.6V, C$_L$=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fc	Serial Clock Frequency For: Dual I/O (BBH), Quad I/O(EBH), Quad Output(6BH) (Dual I/O & Quad I/O Without High Performance Mode), on 3.0V-3.6V power supply			80	MHz
fc1	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O (EBH), Quad Output(6BH) (Dual I/O & Quad I/O Without High Performance Mode), on 2.7V-3.0V power supply			70	MHz
fc2	Serial Clock Frequency For: Dual I/O(BBH), Quad I/O (EBH), Quad Output(6BH) (Dual I/O & Quad I/O With High Performance Mode), on 2.7V-3.6V power supply			80	MHz
fR	Serial Clock Frequency For: Read (03H) Read ID (90H, 9FH and ABH), Read Status Register (05H and 35H)			60	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (Read/Write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0.7			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tCLQV	Clock Low To Output Valid			7	ns
tDP	CS# High To Deep Power-Down Mode			20	μs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			20	μs
tRES2	CS# High To Standby Mode With Electronic Signature Read			20	μs
tSUS	CS# High To Next Command After Suspend			20	μs
tRS	Latency Between Resume And Next Suspend	100			μs
tRST	CS# High To Next Command After Reset(Except From Erase)			30	μs
tRST_E	CS# High To Next Command After Reset (From Erase)			12	ms
tw	Write Status Register Cycle Time		5	40	ms
tBP1	Byte Program Time (First Byte)		30	80	μs
tBP2	Additional Byte Program Time (After First Byte)		2.5	30	μs
tPP	Page Programming Time		0.6	6	ms
tSE	Sector Erase Time (4K Bytes)		50	500	ms

Symbol	Parameter	Min.	Typ.	Max.	Unit.
t_{BE1}	Block Erase Time (32K Bytes)		0.2	2.0	s
t_{BE2}	Block Erase Time (64K Bytes)		0.3	4.0	s
t_{CE}	Chip Erase Time (GD25B32C)		20	80	s

Note:

1. Typical value tested at TA = 25°C.

2. Value guaranteed by design and/or characterization, not 100% tested in production.
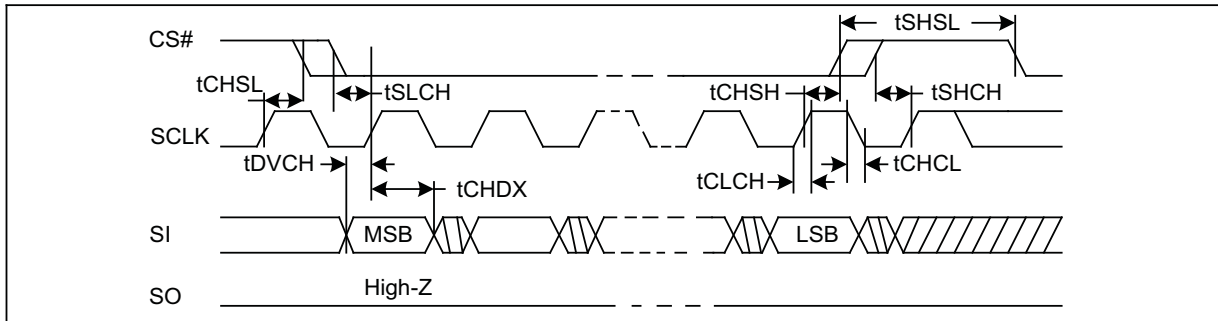
Figure41. Serial Input Timing
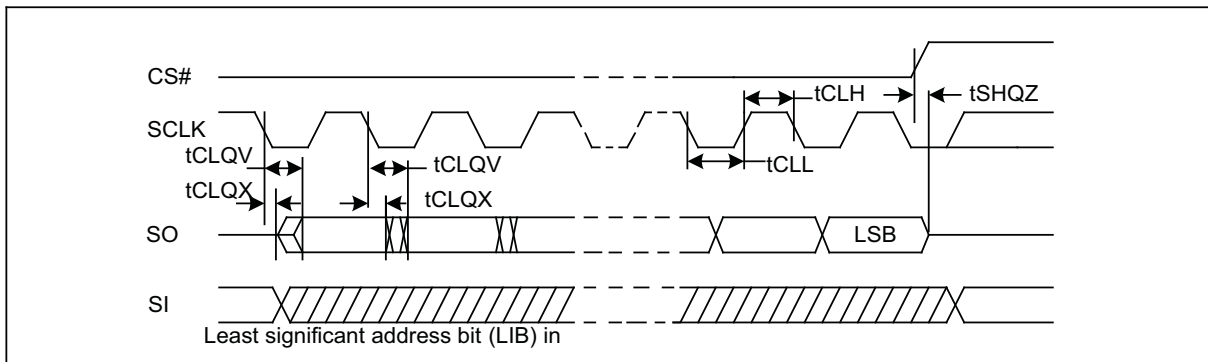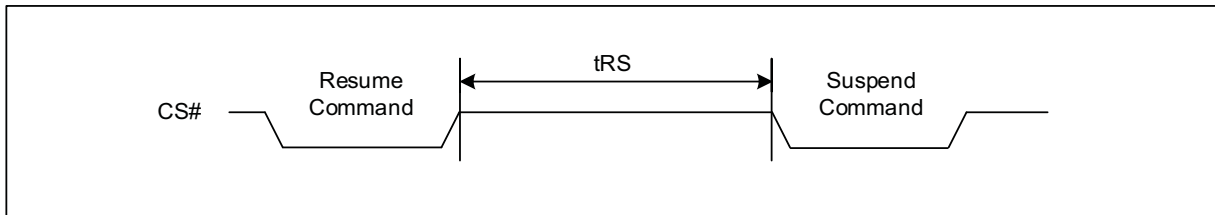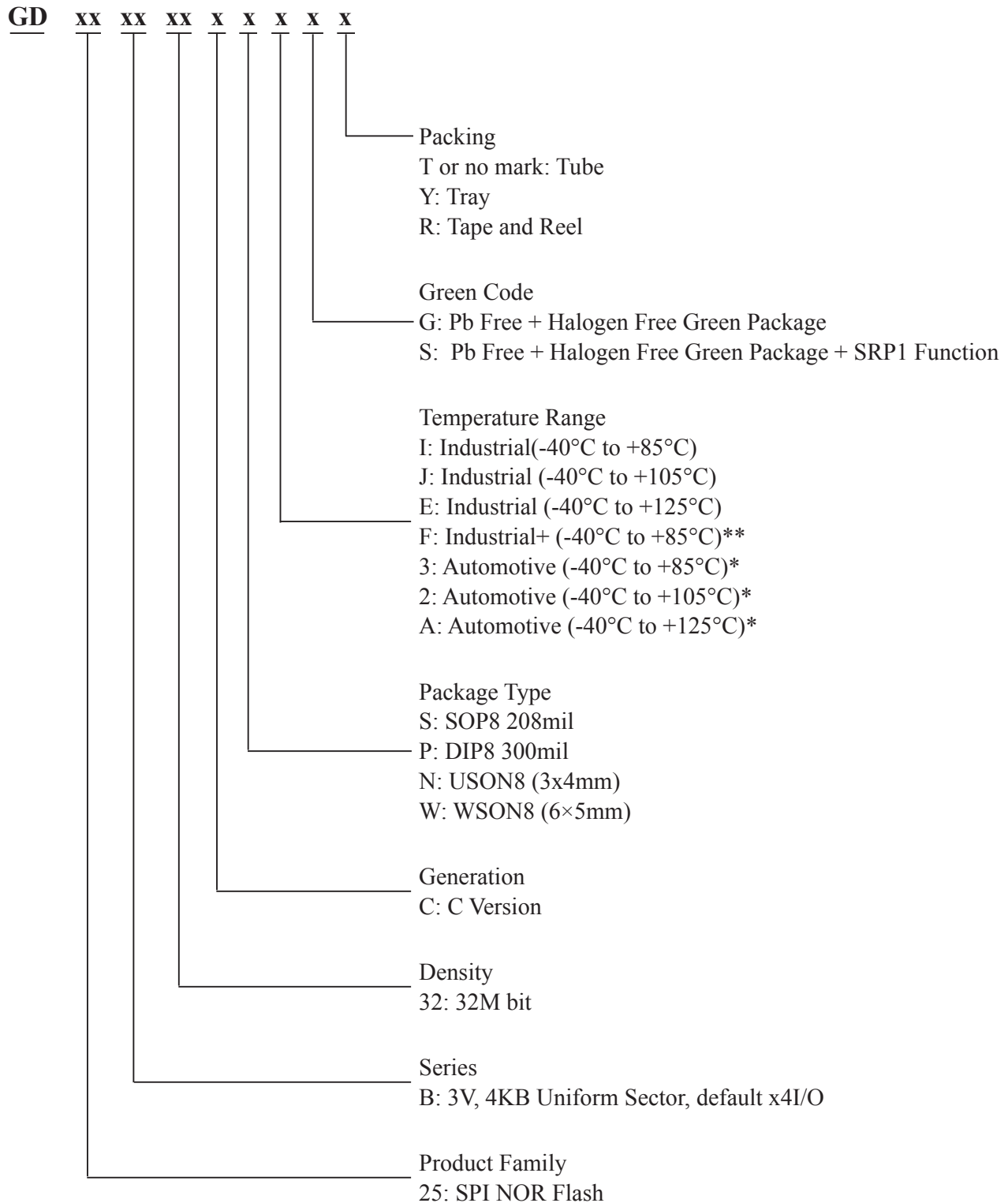

Figure42. Output Timing

Figure43. Resume to Suspend Timing

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9. ORDERING INFORMATION

GD   xx   xx   xx   x   x   x   x   x

Packing
T or no mark: Tube
Y: Tray
R: Tape and Reel

Green Code
G: Pb Free + Halogen Free Green Package
S: Pb Free + Halogen Free Green Package + SRP1 Function

Temperature Range
I: Industrial(-40°C to +85°C)
J: Industrial (-40°C to +105°C)
E: Industrial (-40°C to +125°C)
F: Industrial+ (-40°C to +85°C)**
3: Automotive (-40°C to +85°C)*
2: Automotive (-40°C to +105°C)*
A: Automotive (-40°C to +125°C)*

Package Type
S: SOP8 208mil
P: DIP8 300mil
N: USON8 (3x4mm)
W: WSON8 (6×5mm)

Generation
C: C Version

Density
32: 32M bit

Series
B: 3V, 4KB Uniform Sector, default x4I/O

Product Family
25: SPI NOR Flash

* Please contact GigaDevice sales for automotive products.

** F grade has implemented additional test flows to ensure higher product quality than I grade.

9.1. Valid Part Numbers

Please contact GigaDevice regional sales for the latest product selection and available form factors.

Temperature Range I: Industrial (-40°C to +85°C)

Product Number	Density	Package Type
GD25B32CSIG	32Mbit	SOP8 208mil
GD25B32CSIS		
GD25B32CPIG	32Mbit	DIP8 300mil
GD25B32CPIS		
GD25B32CNIG	32Mbit	USON8 (3x4mm)
GD25B32CNIS		
GD25B32CWIG	32Mbit	WSON8 (6x5mm)
GD25B32CWIS		

Temperature Range J: Industrial (-40°C to +105°C)

Product Number	Density	Package Type
GD25B32CSJG	32Mbit	SOP8 208mil
GD25B32CSJS		
GD25B32CPJG	32Mbit	DIP8 300mil
GD25B32CPJS		
GD25B32CNJG	32Mbit	USON8 (3x4mm)
GD25B32CNJS		
GD25B32CWJG	32Mbit	WSON8 (6x5mm)
GD25B32CWJS		

Temperature Range E: Industrial (-40°C to +125°C)

Product Number	Density	Package Type
GD25B32CSEG	32Mbit	SOP8 208mil
GD25B32CSES		
GD25B32CPEG	32Mbit	DIP8 300mil
GD25B32CPES		
GD25B32CNEG	32Mbit	USON8 (3x4mm)
GD25B32CNES		
GD25B32CWEG	32Mbit	WSON8 (6x5mm)
GD25B32CWES		

Temperature Range F: Industrial (-40°C to +85°C)

Product Number	Density	Package Type
GD25B32CSFG	32Mbit	SOP8 208mil
GD25B32CSFS		
GD25B32CPFG	32Mbit	DIP8 300mil
GD25B32CPFS		
GD25B32CNFG	32Mbit	USON8 (3x4mm)
GD25B32CNFS		
GD25B32CWFG	32Mbit	WSON8 (6x5mm)
GD25B32CWFS		

10. PACKAGE INFORMATION

10.1 Package SOP8 208MIL
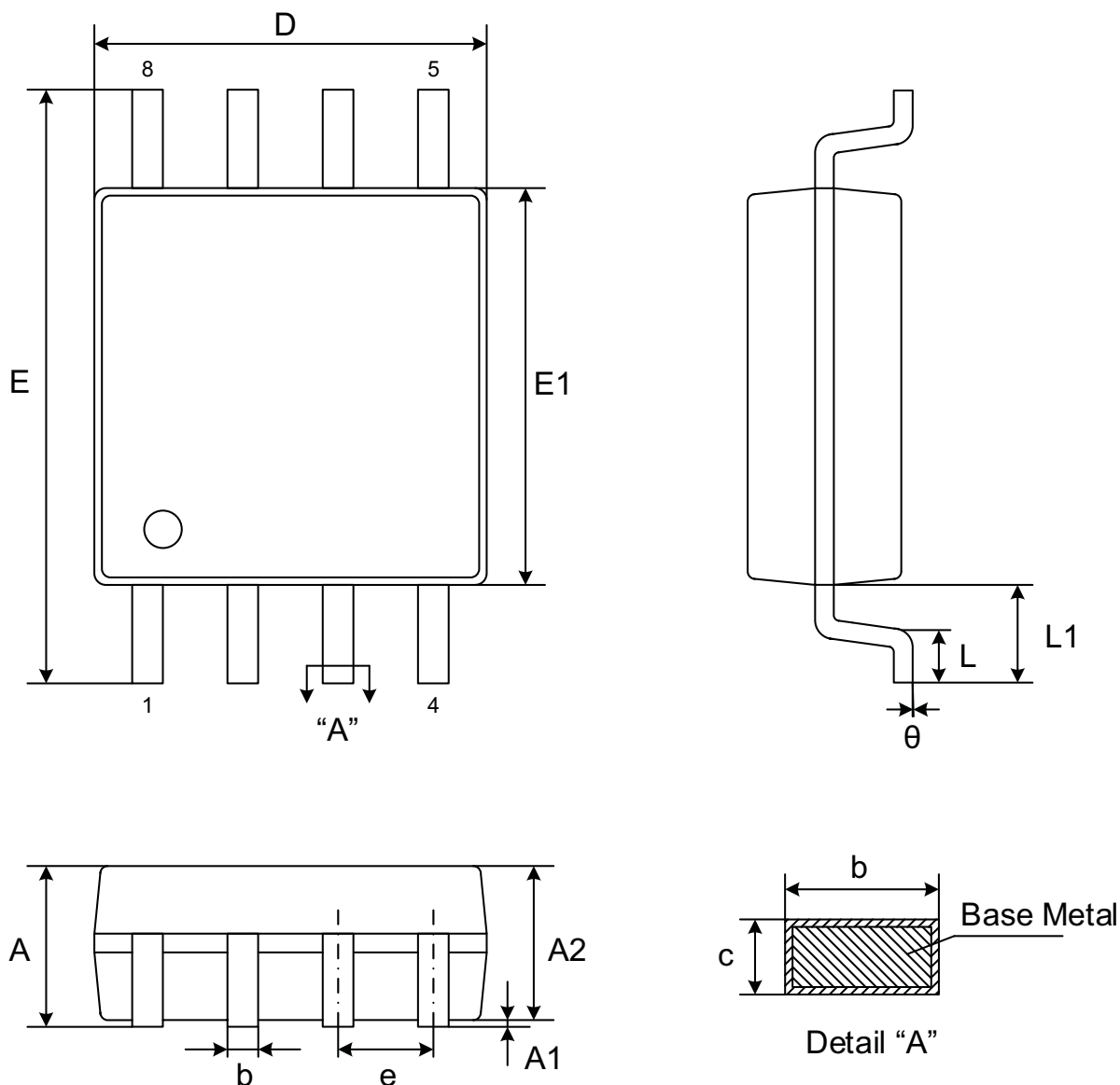
Dimensions

Symbol		A	A1	A2	b	c	D	E	E1	e	L	L1	θ
Unit													
mm	Min	-	0.05	1.70	0.31	0.15	5.13	7.70	5.18	1.27	0.50	1.31	0°
	Nom	-	0.15	1.80	0.41	0.20	5.23	7.90	5.28		-		-
	Max	2.16	0.25	1.90	0.51	0.25	5.33	8.10	5.38		0.85		8°

Note:

1. Both the package length and width do not include the mold flash.
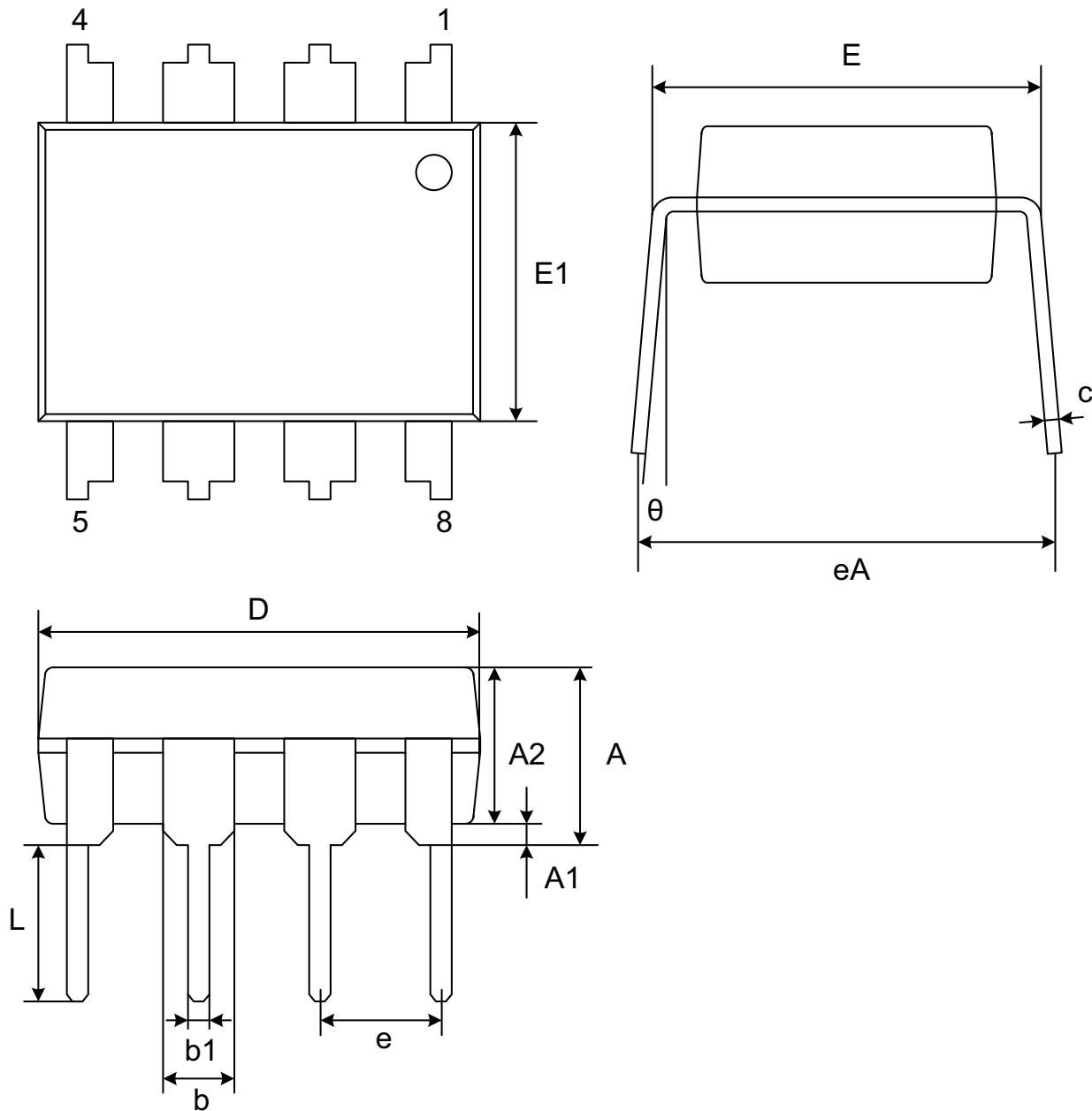
2. Seating plane: Max. 0.1mm.

10.2 Package DIP8 300MIL

Dimensions

Symbol		A	A1	A2	b	b1	C	D	E	E1	e	L	eA	θ
Unit														
mm	Min	-	0.38	3.00	1.14	0.36	0.20	9.02	7.62	6.10	2.54	2.92	8.45	0°
	Nom	-	-	3.30	1.52	0.46	0.25	9.27	7.87	6.35		3.30	8.90	-
	Max	3.88	-	3.50	1.78	0.56	0.35	9.59	8.26	6.60		3.81	9.35	11°

Note: Both the package length and width do not include the mold flash.

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10.3 Package USON8 (3x4mm)

Top View

Side View

Bottom View
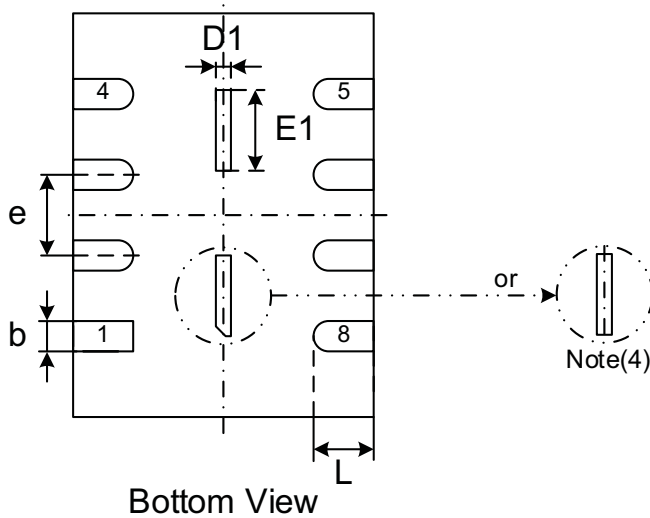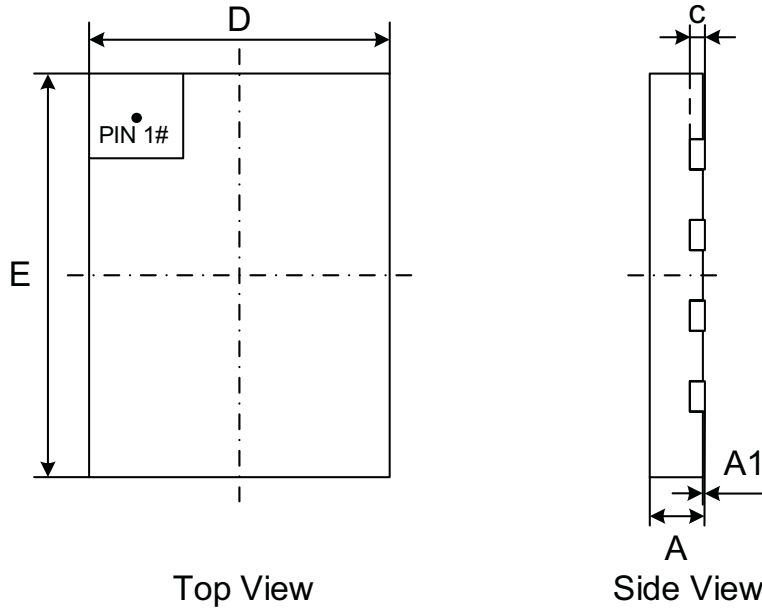
Dimensions

Symbol		A	A1	c	b	D	D1	E	E1	e	L
Unit											
mm	Min	0.50	0.00	0.10	0.25	2.90	0.10	3.90	0.70		0.50
	Nom	0.55	0.02	0.15	0.30	3.00	0.20	4.00	0.80	0.80	0.60
	Max	0.60	0.05	0.20	0.35	3.10	0.30	4.10	0.90		0.70

Note:

1. Both the package length and width do not include the mold flash.

2. The exposed metal pad area on the bottom of the package is floating.

3. Coplanarity ≤0.08mm. Package edge tolerance≤0.10mm.

4. The lead shape may be of little difference according to different package factories. These lead shapes are compatible with each other.

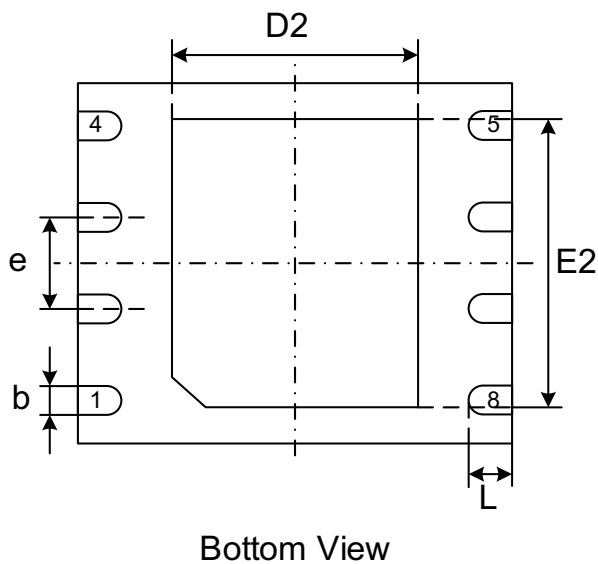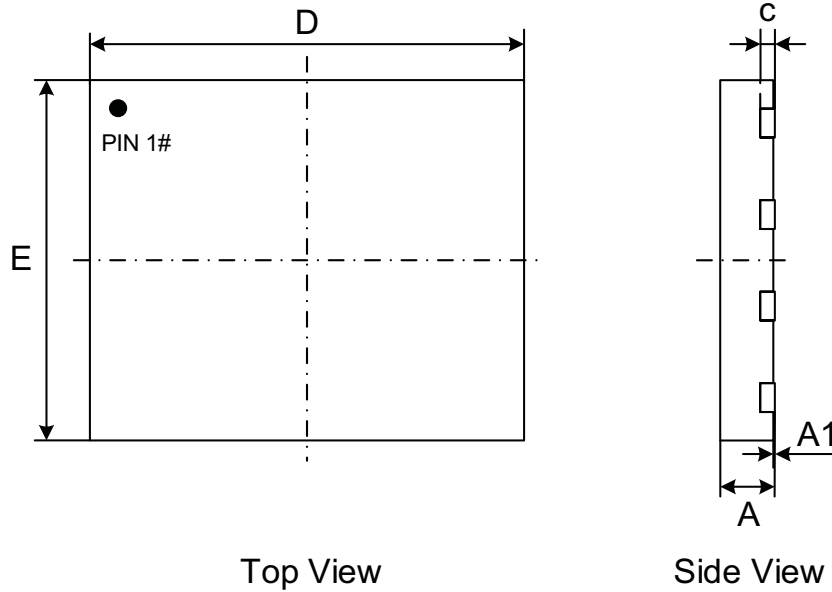http://www.elm-tech.com

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10.4 Package WSON8 (6*5mm)

Top View

Side View

Bottom View

Dimensions

Symbol		A	A1	c	b	D	D2	E	E2	e	L
Unit											
mm	**Min**	0.70	0.00	0.180	0.35	5.90	3.30	4.90	3.90		0.50
	Nom	0.75	0.02	0.203	0.40	6.00	3.40	5.00	4.00	1.27	0.60
	Max	0.80	0.05	0.250	0.50	6.10	3.50	5.10	4.10		0.75

Note:

1. Both the package length and width do not include the mold flash.

11. REVISION HISTORY

Version No	Description	Page	Date
0.0	Initial Preliminary Release	All	2014-10-16
1.0	Initial Release		2014-10-22
1.1	Modify Package WSON 8 (6*5mm)		2015-6-11
1.2	Modify AC CHARACTERISTICS: tCHCL Min.0.2 V/ns Change to 0.1 V/ns tCLCH Min.0.2 V/ns Change to 0.1 V/ns Modify POWER-ON TIMING		2015-11-17
1.3	Modify AC CHARACTERISTICS: add tRST_R & tRST_P & tRST_E Modify POWER-ON TIMING: TVSL Min 10us Change to 5ms		2015-12-18
1.4	Modify Package SOP8		2016-5-13
1.5	Modify tVSL from 5ms to 1.8ms Modify VWI from 1~2.5V to 1.5~2.5V Modify ICC4 –ICC8 from 20mA to 25mA Modify ICC9 from 400~700uA to 0.6~1.2mA Add tRS, of which the min value is100us Delete tRST_P and tRST_E. Add tRST, of which the max value is 30us Update the description of all packages Add "Page" column to the Revision History		2018-5-21
1.6	Add 4BH command Modify the sequence diagram of 42H command Modify Ordering Information		2018-9-11
1.7	Modify tSE max value from 200/300ms to 300ms Modify tBE1 max value from 0.8/1.6s to 1.6s Modify tBE2 max value from 1.2/2.0s to 2.0s		2018-12-4
1.8	Update Ordering Information		2019-6-3
1.9	Add AC/DC CHARACTERISTICS @-40°C~105°C@-40°C~125°C Update Ordering Information		2019-8-2
2.0	Update Ordering Information		2019-9-9

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