

Complementary MOSFET

ELM4C4903FKA-N

<http://www.elm-tech.com>

■General description

ELM4C4903FKA-N uses advanced trench technology to provide excellent $R_{ds(on)}$, low gate charge and low gate threshold voltage.

■Features

N-channel

- $V_{ds}=40V$
- $I_d=23A$ ($V_{gs}=10V$)
- $R_{ds(on)} = 28m\Omega$ ($V_{gs}=10V$)
- $R_{ds(on)} = 42m\Omega$ ($V_{gs}=4.5V$)

P-channel

- $V_{ds}=-40V$
- $I_d=-20A$ ($V_{gs}=-10V$)
- $R_{ds(on)} = 40m\Omega$ ($V_{gs}=-10V$)
- $R_{ds(on)} = 65m\Omega$ ($V_{gs}=-4.5V$)

■Maximum absolute ratings

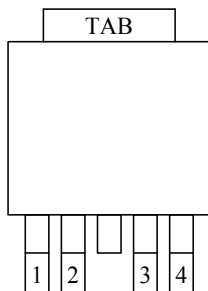
Parameter		Symbol	N-ch (Max.)	P-ch (Max.)	Unit	Note
Drain-source voltage		V_{ds}	40	-40	V	
Gate-source voltage		V_{gs}	± 20	± 20	V	
Continuous drain current ($V_{gs}=10$)	$T_c=25^{\circ}C$	I_d	23	-20	A	1
	$T_c=100^{\circ}C$		18	-16		
Pulsed drain current		I_{dm}	46	-40	A	2
Single pulse avalanche energy		EAS	28	66	mJ	3
Avalanche current		I_{as}	17.8	-27.2	A	
Power dissipation	$T_c=25^{\circ}C$	P_d	25.0	31.3	W	4
Storage temperature range		T_{stg}	-55 to 150	-55 to 150	$^{\circ}C$	
Operating junction temperature range		T_j	-55 to 150	-55 to 150	$^{\circ}C$	

■Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Note
Thermal resistance junction-to-ambient	$R_{\theta ja}$	-	62	$^{\circ}C/W$	1
Thermal resistance junction-case	$R_{\theta jc}$	-	5	$^{\circ}C/W$	1

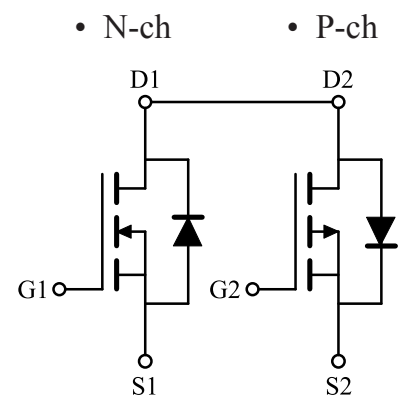
■Pin configuration

TO-252-4(TOP VIEW)



Pin No.	Pin name
1	SOURCE1
2	GATE1
3	SOURCE2
4	GATE2
TAB	DRAIN1/DRAIN2

■Circuit



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■Electrical characteristics (N-ch)

Tj=25°C. Unless otherwise noted.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
STATIC PARAMETERS							
Drain-source breakdown voltage	BV _{dss}	V _{gs} =0V, I _d =250μA	40	-	-	V	
Static drain-source on-resistance	R _{ds(on)}	V _{gs} =10V, I _d =12A	-	-	28	mΩ	2
		V _{gs} =4.5V, I _d =10A	-	-	42		
Gate threshold voltage	V _{gs(th)}	V _{gs} =V _{ds} , I _d =250μA	1.0	1.5	2.5	V	
Zero gate voltage drain current	I _{dss}	V _{ds} =32V, V _{gs} =0V	-	-	1	μA	
		V _{ds} =32V, V _{gs} =0V, Tj=55°C	-	-	5		
Gate-body leakage current	I _{gss}	V _{gs} =±20V, V _{ds} =0V	-	-	±100	nA	
Forward transconductance	G _{fs}	V _{ds} =5V, I _d =12A	-	8	-	S	
Max. body-diode continuous current	I _s	V _{gs} =V _{ds} =0V, Force current	-	-	23	A	1, 5
Pulsed source current	I _{sm}		-	-	46	A	2, 5
Diode forward voltage	V _{sd}	V _{gs} =0V, I _s =1A	-	-	1.2	V	2
DYNAMIC PARAMETERS							
Input capacitance	C _{iss}	V _{ds} =15V, V _{gs} =0V, f=1MHz	-	593	-	pF	
Output capacitance	C _{oss}		-	76	-	pF	
Reverse transfer capacitance	C _{rss}		-	56	-	pF	
Gate resistance	R _g	V _{ds} =0V, V _{gs} =0V, f=1MHz	-	2.6	5.2	Ω	
SWITCHING PARAMETERS							
Total gate charge (4.5V)	Q _g	V _{ds} =20V, V _{gs} =4.5V I _d =12A	-	5.50	-	nC	
Gate-source charge	Q _{gs}		-	1.25	-	nC	
Gate-drain charge	Q _{gd}		-	2.50	-	nC	
Turn-on delay time	t _{d(on)}	V _{ds} =20V, V _{gs} =10V R _{gen} =3.3Ω, I _d =1A	-	8.9	-	ns	
Turn-on rise time	t _r		-	2.2	-	ns	
Turn-off delay time	t _{d(off)}		-	41.0	-	ns	
Turn-off fall time	t _f		-	2.7	-	ns	

NOTE :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs and duty cycle ≤ 2%.
3. The EAS data shows Max. rating . The test condition is V_{dd}=25V, V_{gs}=10V, L=0.1mH, I_{as}=17.8A.
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_d and I_{dm}, in real applications, should be limited by total power dissipation.

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■ Typical electrical and thermal characteristics (N-ch)

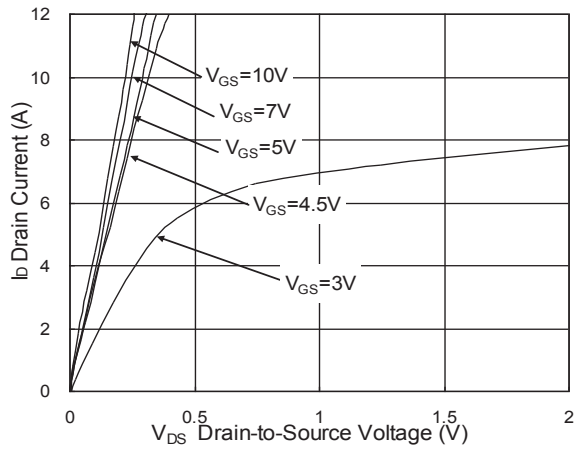


Fig.1 Typical Output Characteristics

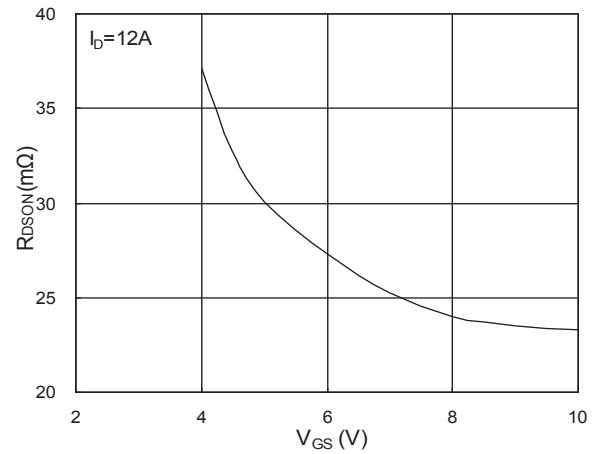


Fig.2 On-Resistance vs. G-S Voltage

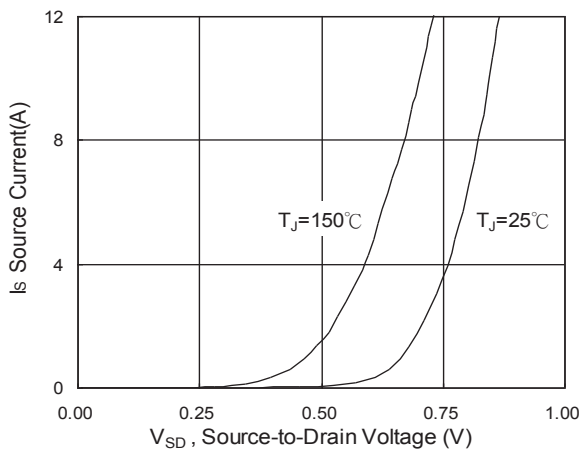


Fig.3 Forward Characteristics of Reverse

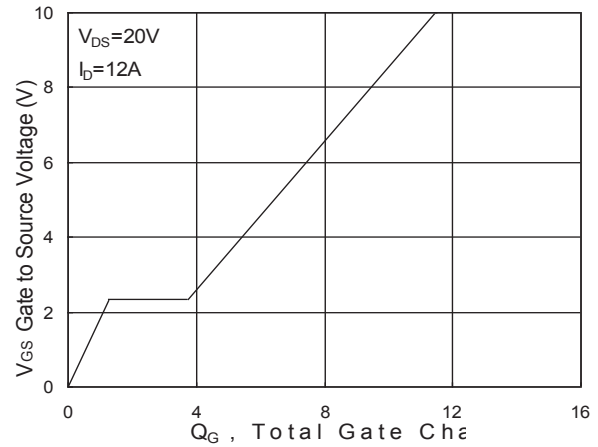


Fig.4 Gate-Charge Characteristics

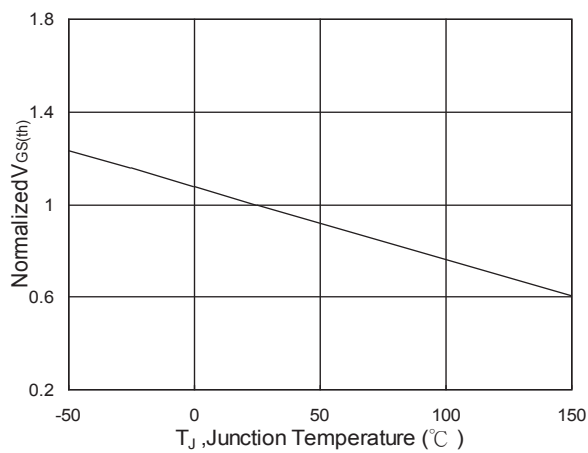


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

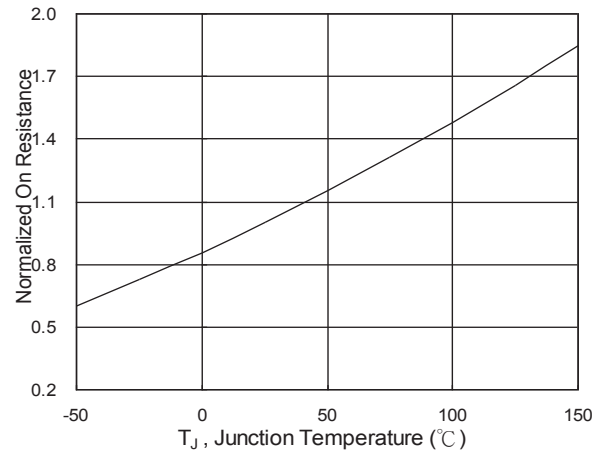


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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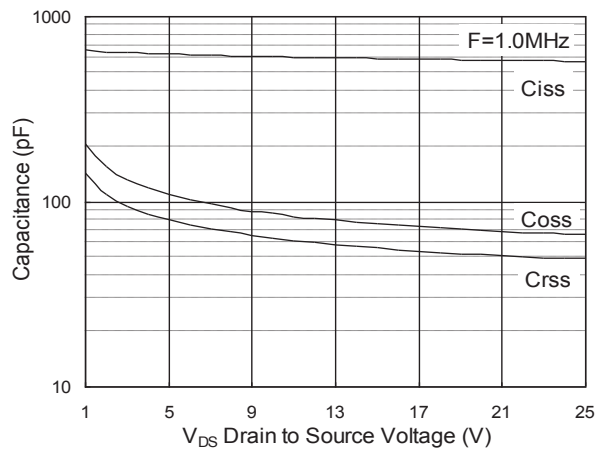


Fig.7 Capacitance

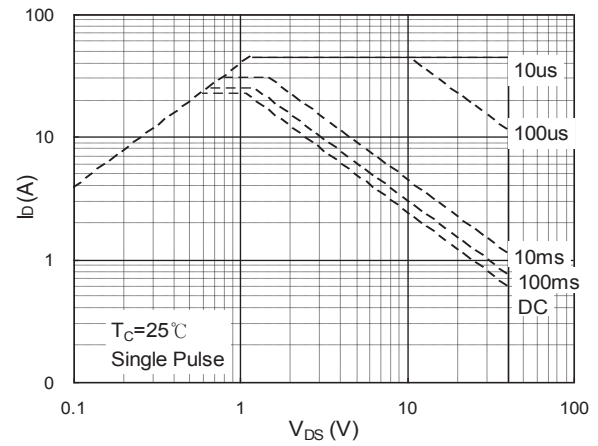


Fig.8 Safe Operating Area

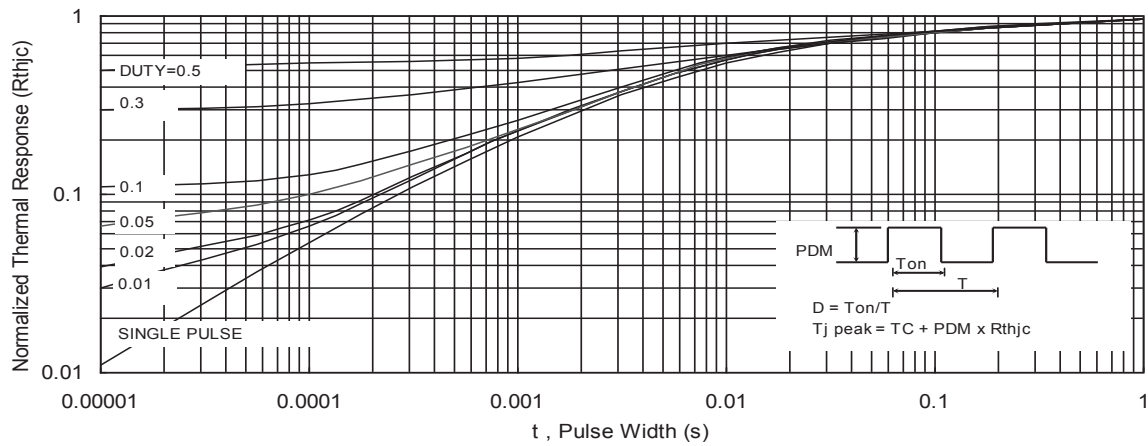


Fig.9 Normalized Maximum Transient Thermal Impedance

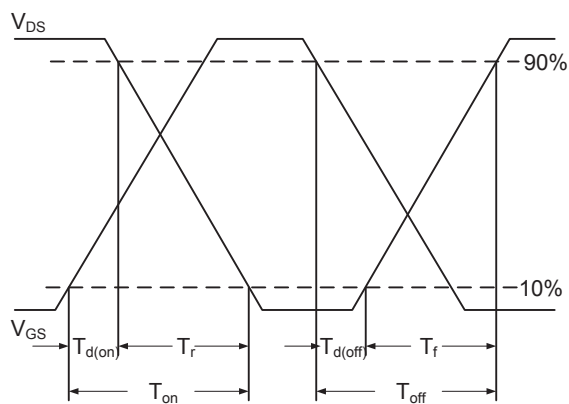


Fig.10 Switching Time Waveform

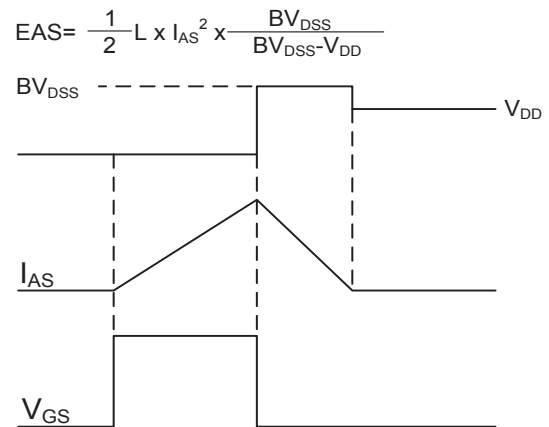


Fig.11 Unclamped Inductive Switching Wave

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■Electrical Characteristics (P-ch)

T_j=25°C. Unless otherwise noted.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
STATIC PARAMETERS							
Drain-source breakdown voltage	BV _{dss}	V _{gs} =0V, I _d =-250μA	-40	-	-	V	
Static drain-source on-resistance	R _{ds(on)}	V _{gs} =-10V, I _d =-8A	-	-	40	mΩ	2
		V _{gs} =-4.5V, I _d =-4A	-	-	65		
Gate threshold voltage	V _{gs(th)}	V _{gs} =V _{ds} , I _d =-250μA	-1.0	-1.6	-2.5	V	
Zero gate voltage drain current	I _{dss}	V _{ds} =-32V, V _{gs} =0V	-	-	-1	μA	
		V _{ds} =-32V, V _{gs} =0V, T _j =55°C	-	-	-5		
Gate-body leakage current	I _{gss}	V _{gs} =±20V, V _{ds} =0V	-	-	±100	nA	
Forward transconductance	G _{fs}	V _{ds} =-5V, I _d =-8A	-	12.6	-	S	
Max. body-diode continuous current	I _s	V _{gs} =V _{ds} =0V, Force current	-	-	-20	A	1, 5
Pulsed source current	I _{sm}		-	-	-40	A	2, 5
Diode forward voltage	V _{sd}	V _{gs} =0V, I _s =-1A	-	-	-1	V	2
DYNAMIC PARAMETERS							
Input capacitance	C _{iss}	V _{ds} =-15V, V _{gs} =0V, f=1MHz	-	1004	-	pF	
Output capacitance	C _{oss}		-	108	-	pF	
Reverse transfer capacitance	C _{rss}		-	80	-	pF	
Gate resistance	R _g	V _{ds} =0V, V _{gs} =0V, f=1MHz	-	13	16	Ω	
SWITCHING PARAMETERS							
Total gate charge (-4.5V)	Q _g	V _{ds} =-20V, V _{gs} =-4.5V I _d =-12A	-	9.00	-	nC	
Gate-source charge	Q _{gs}		-	2.54	-	nC	
Gate-drain charge	Q _{gd}		-	3.10	-	nC	
Turn-on delay time	t _{d(on)}	V _{ds} =-15V, V _{gs} =-10V R _{gen} =3.3Ω, I _d =-1A	-	19.2	-	ns	
Turn-on rise time	t _r		-	12.8	-	ns	
Turn-off delay time	t _{d(off)}		-	48.6	-	ns	
Turn-off fall time	t _f		-	4.6	-	ns	

NOTE :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs and duty cycle ≤ 2%.
3. The EAS data shows Max. rating . The test condition is V_{dd}=-25V, V_{gs}=-10V, L=0.1mH, I_{as}=-27.2A.
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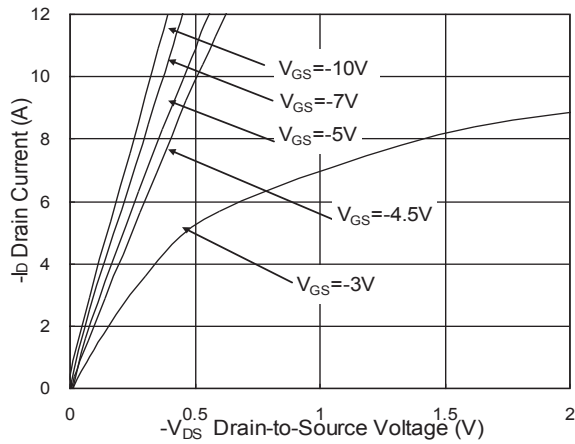


Fig.1 Typical Output Characteristics

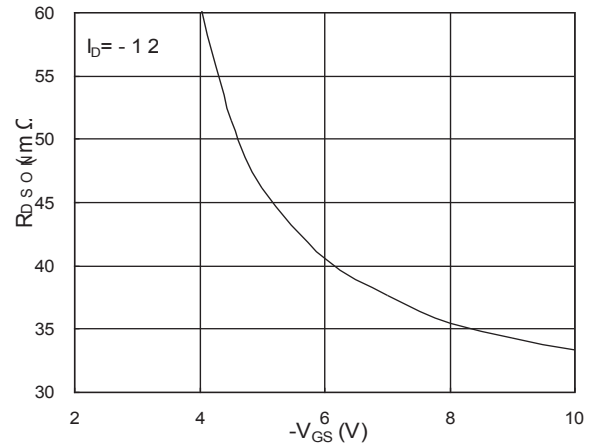


Fig.2 On-Resistance v.s Gate-Source

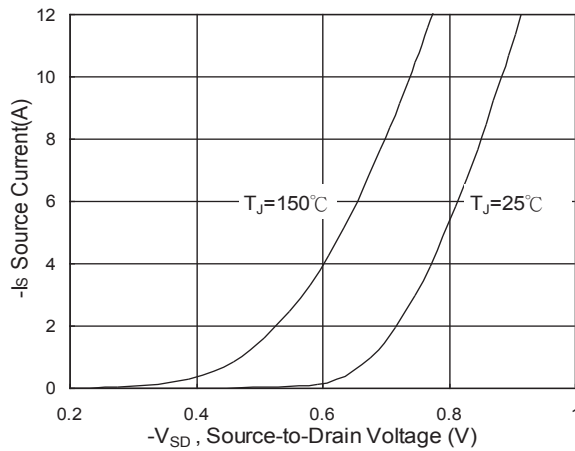


Fig.3 Forward Characteristics of Reverse

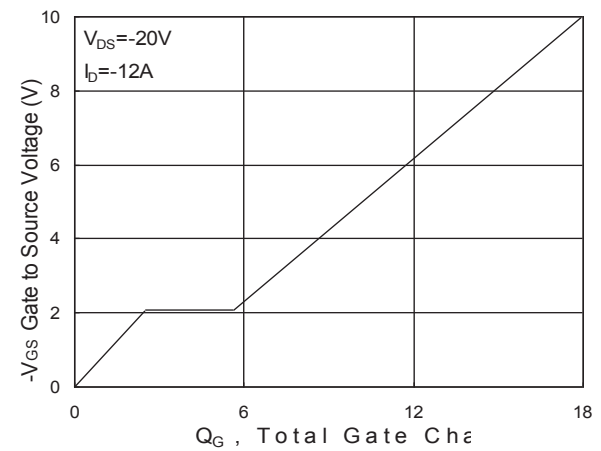


Fig.4 Gate-Charge Characteristics

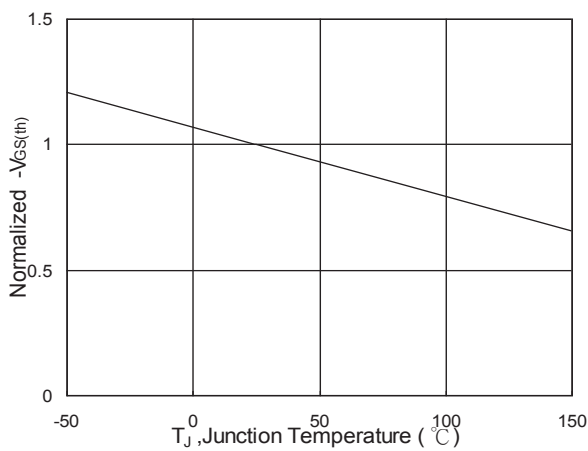


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

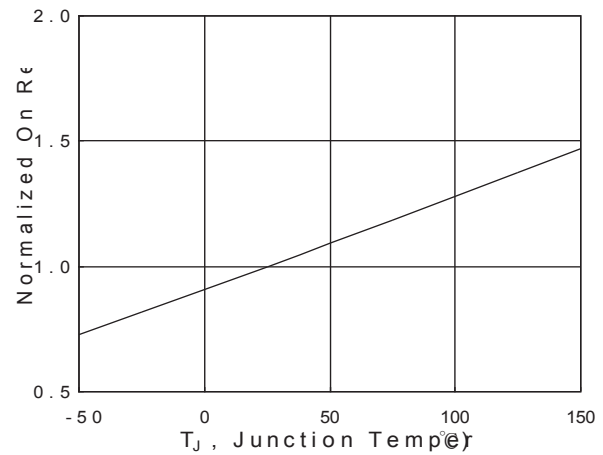


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

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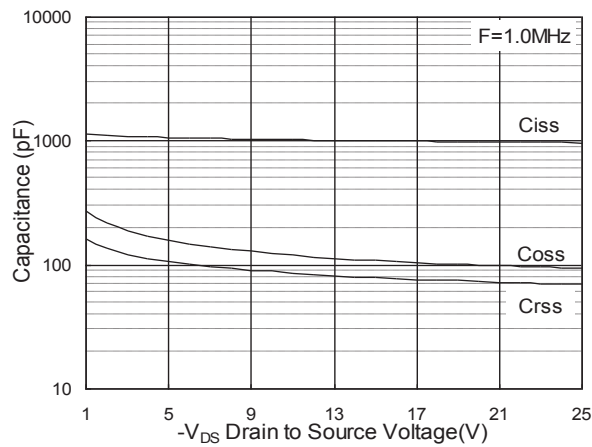


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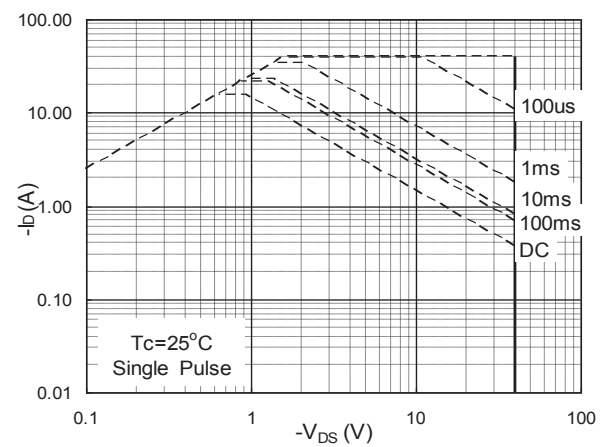


Fig.8 Safe Operating Area

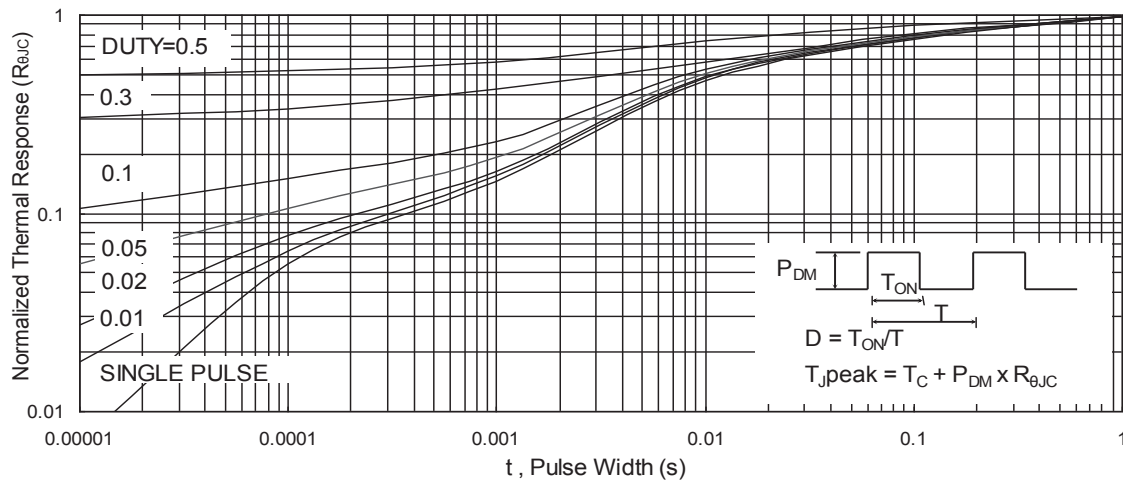


Fig.9 Normalized Maximum Transient Thermal Impedance

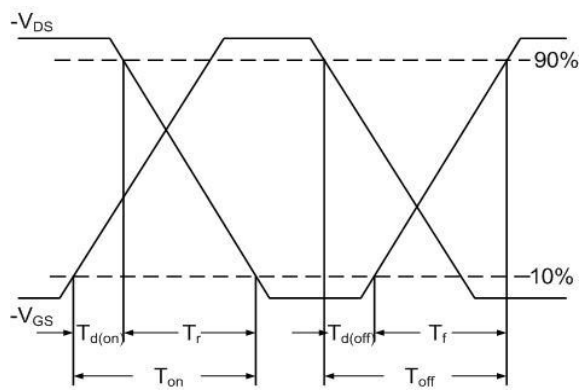


Fig.10 Switching Time Waveform

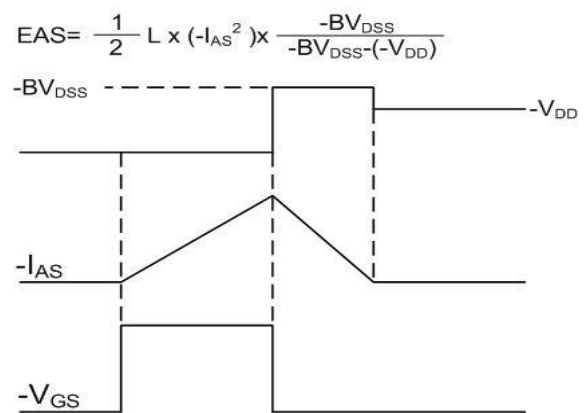


Fig.11 Unclamped Inductive Waveform